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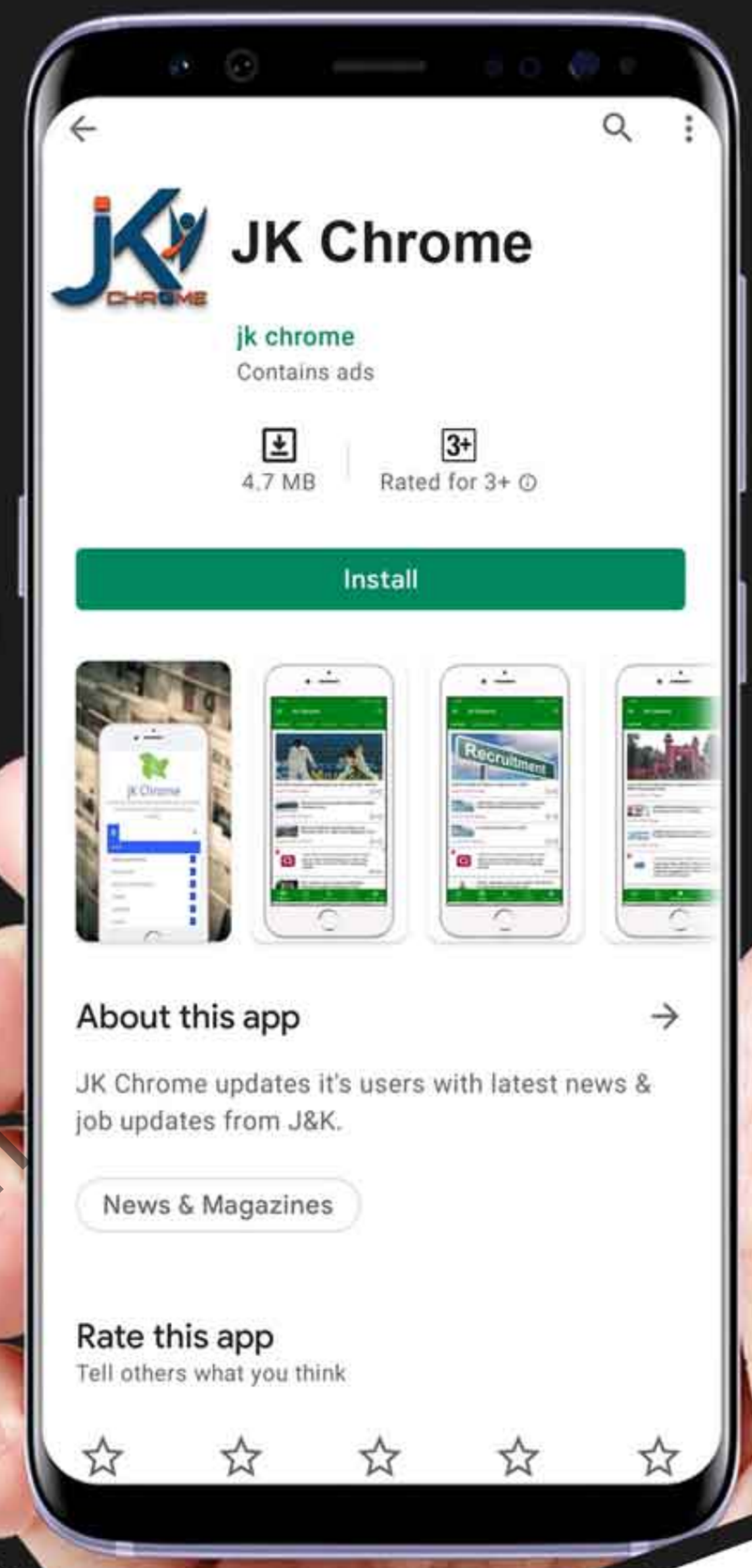

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EDC & Analog Electronics

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Diode Types & its Applications

EDC & Analog Electronics: Diode Types & its Applications

Clipper Circuits

Diode network that have the ability to clip of a portion of the input signal without distorting the remaining part of the alternating waveform is known as Clipper.

There are two general categories of clippers

1. Series clipper
2. Parallel Clipper

The series configuration is defined as one where the diode is in series with the load, while the parallel configuration has the diode in a branch parallel to the load.

(a) Series Clipper

(i) Unbiased Clipper

The response of series configuration of figure 1(a) to a variety of alternating waveform is provided in figure 1(b)

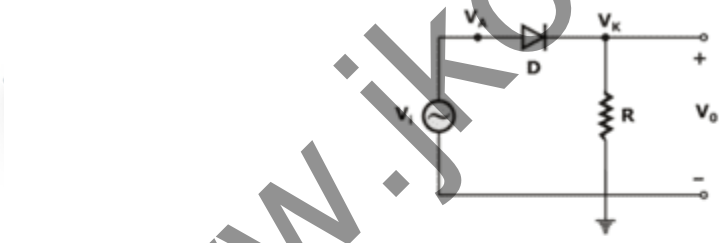


Figure 1(a)

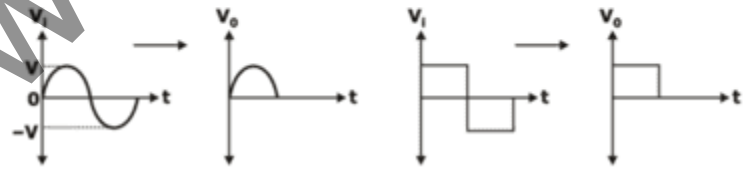


Figure 1(b)

From figure 1(a), Anode voltage of diode $V_A = V_i$ and Cathode voltage $V_K = 0$

Therefore, for positive half cycle $V_A > V_K$, which means diode is forward biased and act as short circuit.

For negative half cycle $V_A < V_K$, which means diode is reverse biased and act as open circuits.

(ii) Biased clipper

The addition of a dc supply that can have a pronounced effect on the output of a clipper is shown in figure 2.

NOTE: Make a mental sketch of the response of the network based on the direction of the diode and the applied voltage levels.

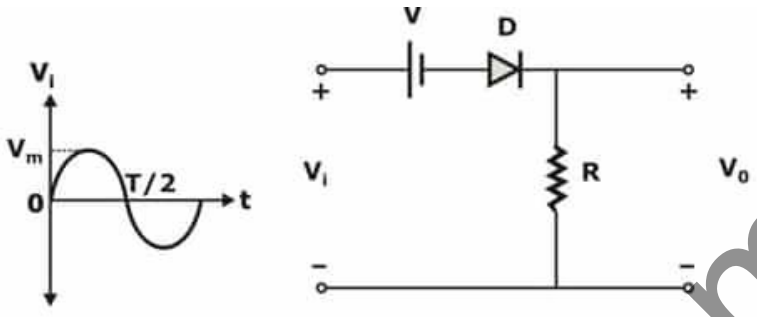


Figure 2: Series clipper with a dc supply

For the given network, the direction of diode suggest that the signal V_i must be positive to turn it ON. The dc supply further requires that the voltage V_i be greater than V to turn ON the diode. The negative region of the input signal is pressuring the diode into the OFF state, supported further by the dc supply.

NOTE: Determine the applied voltage (transition voltage) that will cause a change in state for the diode.

For the ideal diode the transition between states will occur on the characteristics, where $V_d = 0$ V and $i_d = 0$A. Applying the condition $i_d = 0$ at $V_d = 0$ to the network of figure 2 will result in the configuration of figure 3(a), where it is recognized that the level of V_i that will cause a transition in state is $V_i = V$

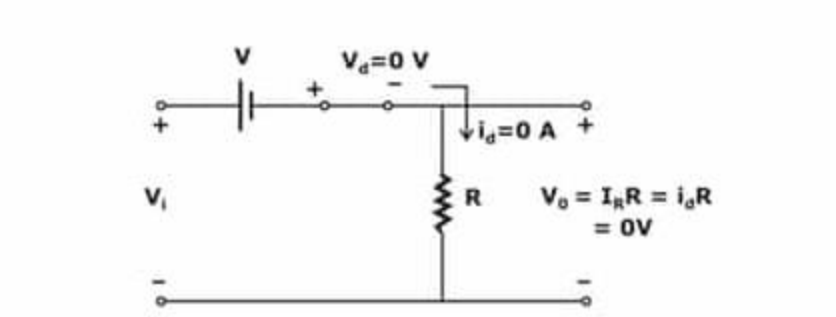


Figure 3(a): Determining the transition level for the circuit of figure 2.

For an input voltage greater than V volts the diode is in the short circuit state, while input voltage less than V volts it is in the open circuit or off state.

NOTE: Be continually aware of the defined terminals and polarity of V_0.

When the diode is in the short circuit state, such as shown in figure 4, the output voltage V_0 can be determined by applying KVL in the clockwise direction.

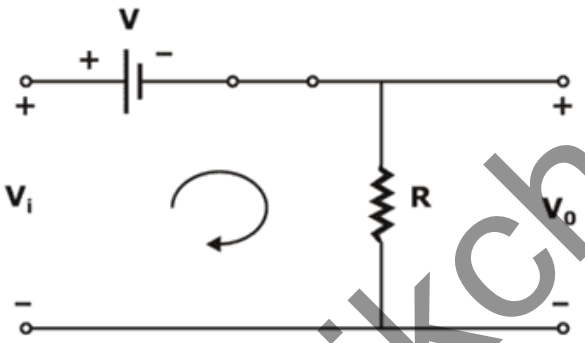


Figure 4

$V_i - V - V_0 = 0$

$\therefore V_0 = V_i - V$

NOTE: It can be helpful to sketch the input signal above the output and determine the output and determine the output at instantaneous values of the input.

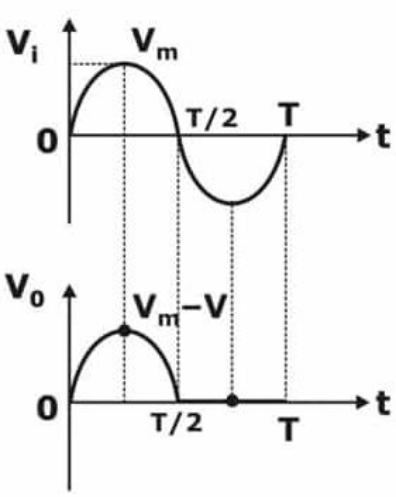


Figure 5

For an instantaneous value of V_i the input can be treated as a dc supply of that value and corresponding dc value of the output determined.

For instant at $V_i = V_m$

For $V_m > V$, diode is short circuit and $V_0 = V_m - V$

When diode change state, and $V_i = -V_m$

Then $V_0 = 0$ V

And now complete the curve for V_0 that can be shown in figure 5.

(b) Parallel Clipper

The network of figure 6 is the simplest of parallel diode configuration with the output for the same input as discussed earlier. The analysis of parallel configuration is very similar to that applied to series configurations.

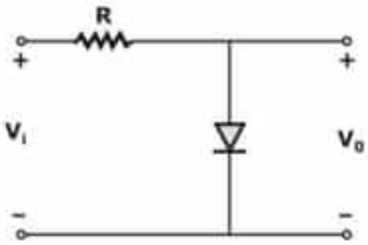


Figure 6: Parallel clipper circuits

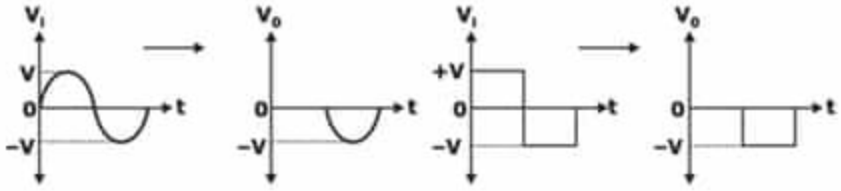
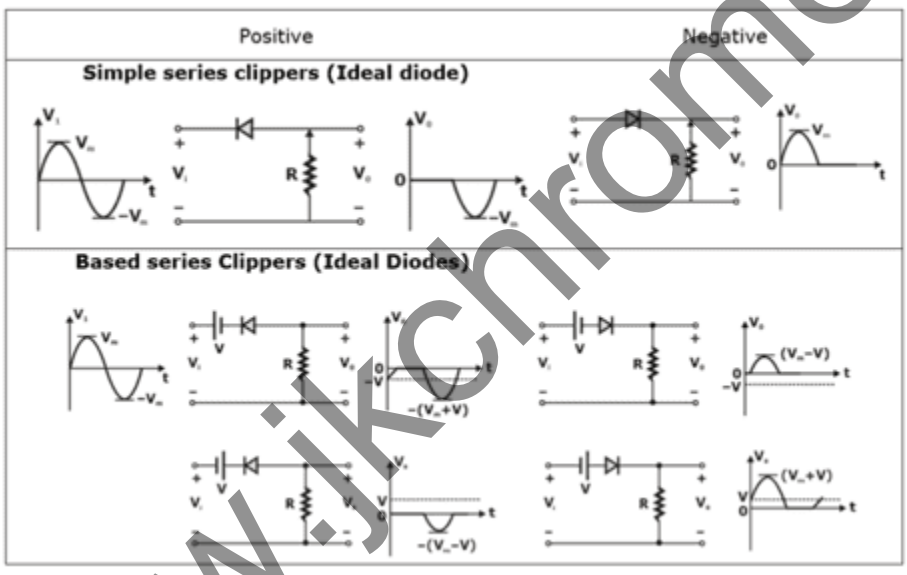


Figure 7: Response of parallel Clipper.

Summary of Series & Parallel Clipper

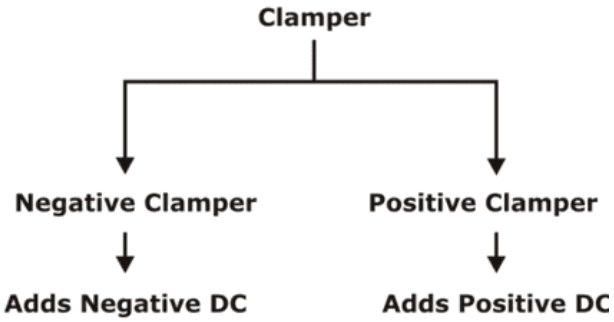


Clampers

The clamping network is one that will clamp a signal to a different dc level. The network consist of a capacitor, a diode and a resistor element and an independent dc supply to introduce on additional shift.

The magnitude of R and C must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is non conducting.

There are basically two type of clamper:



(a) Negative Clamper

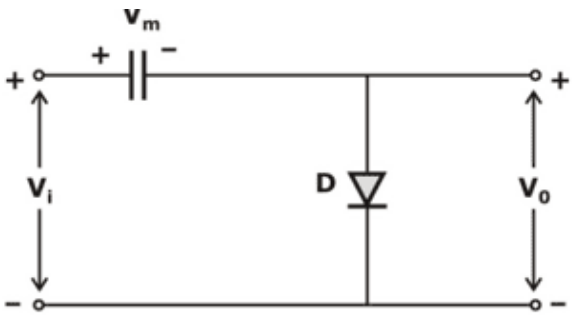


Figure 8(a): Ideal clamper circuit

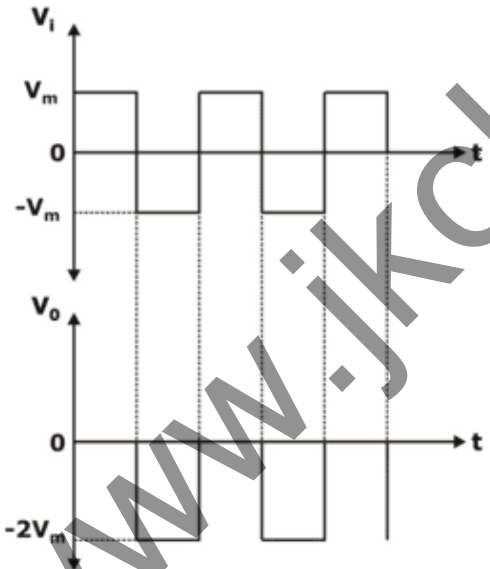


Figure 8(b): Waveform

When the input is positive, diode operates in forward bias and capacitor charge through diode. If diode is ideal it behaves as short circuit and therefore capacitor charge up to the peak input V_m.

When input becomes negative, capacitor should discharge but discharge path is not available so capacitor voltage will continue to remain V_m. Therefore, once capacitor is fully charged its voltage V_m irrespective of the input being positive or negative.

Applying KVL

$$-V_i + V_m + V_0 = 0$$

$$V_0 = V_i - V_m$$

$$= V_i + (-V_m)$$

Hence circuit adds dc voltage of $-V_m$. So, the output will be a square waveform for given input whose value varies from 0 to $-2V_m$.

Positive peak of output waveform touches 0V level or positive peak gets clamped to 0V. Since a negative clamper is clamping positive peak to 0V so it is called positive peak clamper.

NOTE: If diode has cut in voltage V_γ then it should be replaced with series connection of ideal diode and battery V_γ.

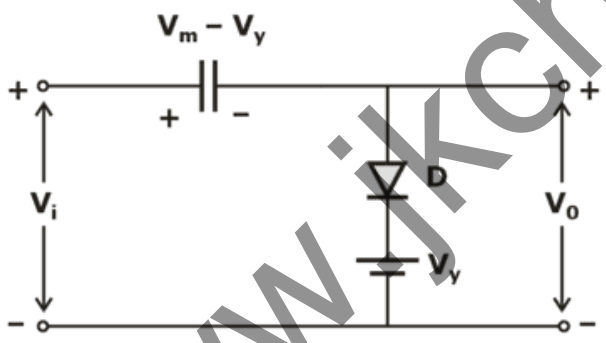


Figure 9(a)

When input is +Ve, capacitor changes through diode upto a maximum voltage of $V_m - V_\gamma$

$\therefore\ V_0 = V_i = (V_m - V_\gamma)$

$$V_0 = V_i + (-V_m + V_\gamma)$$

Hence circuit add dc voltage equal to $-(V_m - V_\gamma)$

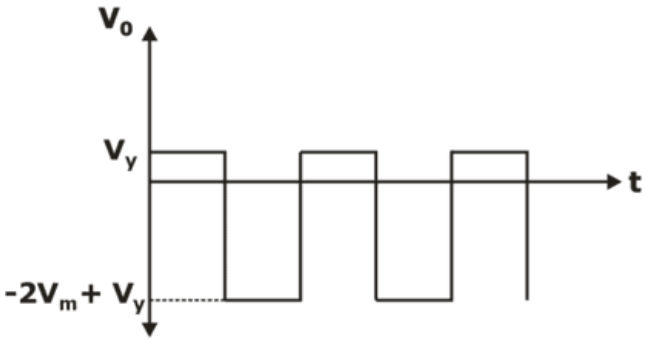


Figure 9(b): Waveform

(b) Positive Clamper

- When input is negative diode gets forward biased and capacitor charges through diode up to peak input V_m
- When input becomes positive capacitor will not be able to discharge as discharge path is not present. Therefore, voltage across the capacitor remains V_m irrespective of input being $+V_m$ or $-V_m$

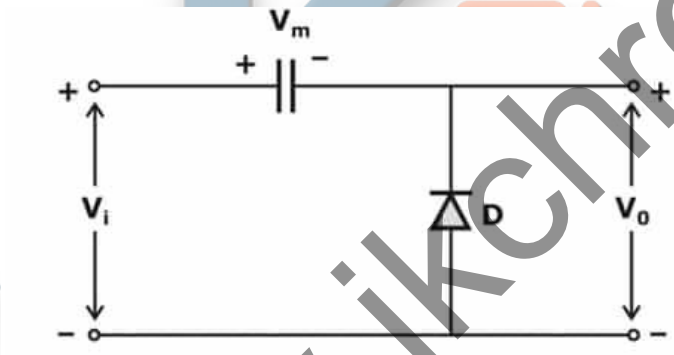


Figure 10(a): Positive clamper circuit

Applying KVL

$V_0 = V_i + V_m$

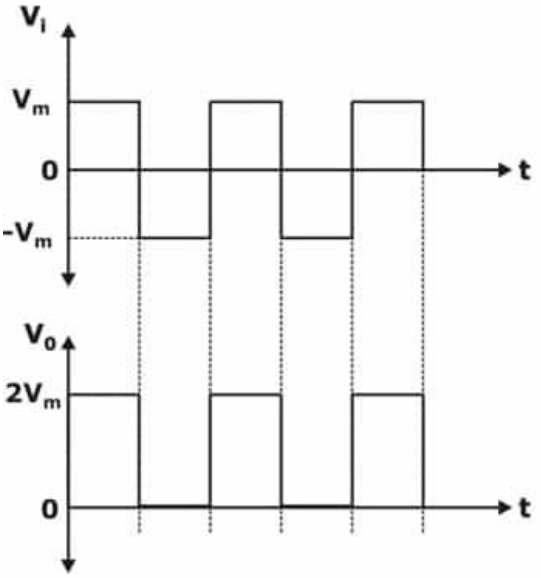


Figure 10(b): Waveform

Negative peak output gets clamped to 0 volts therefore positive clamper is also called negative clamper.

NOTE: It diode has cut in voltage V_γ then capacitor changes to a voltage ($V_m - V_\gamma$)

$\therefore V_0 = V_i + (V_m - V_\gamma)$

Hence added dc voltage is $V_m - V_\gamma$

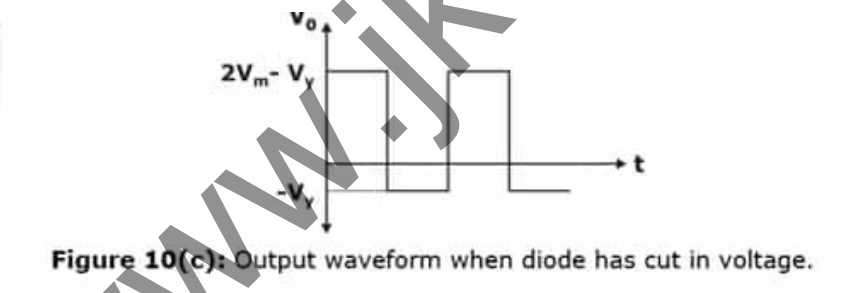


Figure 10(c): Output waveform when diode has cut in voltage.

REGULATOR

- The most important property for an ideal power supply is to maintain a constant voltage at the output terminals for all operating conditions.

- But practically there is a drop-in output terminal voltage of the power supply as the load current increases, so we require to regulate the power at optimum level using a voltage regulator.

Performance Parameters of a Good Voltage Regulator

- **Load Regulation Factor**

It is the change in the load voltage from no load to full load.

- **Line Regulation Factor**

It is the effect of variations in the supply voltage causing variations in the output voltage of the regulator.

$$\%\ \text{Line Regulation} = \left(\frac{\text{Change in } V_o \text{ at } V_{imin} \text{ to } V_{imax}}{V_{oFL}}\right) \times 100 = \left(\frac{V_{01} - V_{02}}{V_{o(nominal)}}\right) \times 100$$

V_{01} is the output voltage at the maximum input voltage while V_{02} is the output voltage at the minimum input voltage.

Zener Diode

- Zener diode is a special purpose diode designed to operate under reverse bias in the breakdown region.
- A Zener diode has higher doping than conventional diodes
- In a Zener diode the depletion layer is very thin and electric field strength at the junction is very high even for a small reverse voltage.

Application of Zener Diode as a Voltage Regulator

- At the instant when the applied reverse biased voltage on the Zener diode is equal to the Zener breakdown voltage, further increase in reverse voltage makes the electric field at the p-n junction significantly high.
- The electric field is high enough to pull the electrons that are beyond the junction on the n-side towards the p-side, significantly increasing the current.

- The increased current allows a wide range of current to flow through the diode in the breakdown region such that the reverse voltage has no significant change.

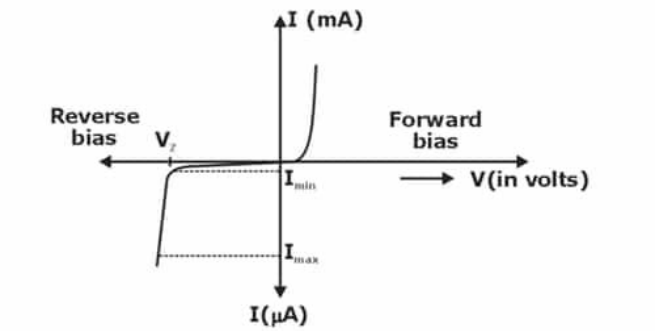


Figure 7: i-v Characteristics of Zener Diode

Equivalent Circuit of Zener Diode

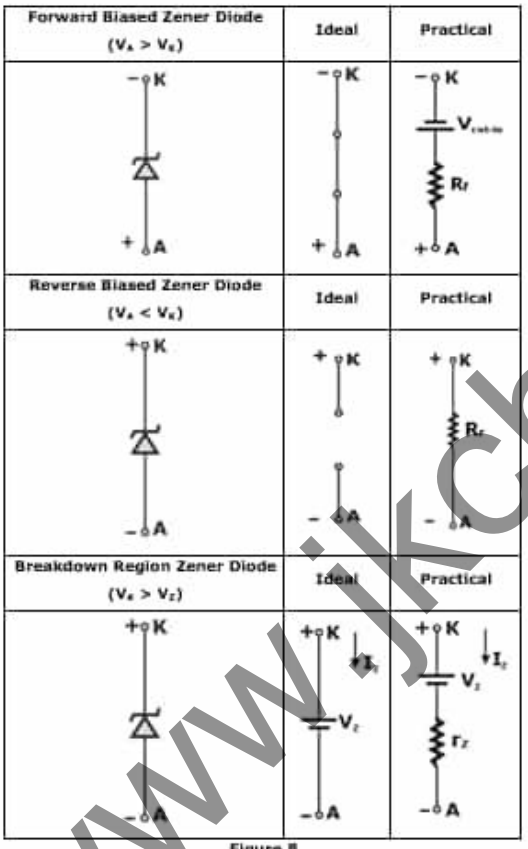


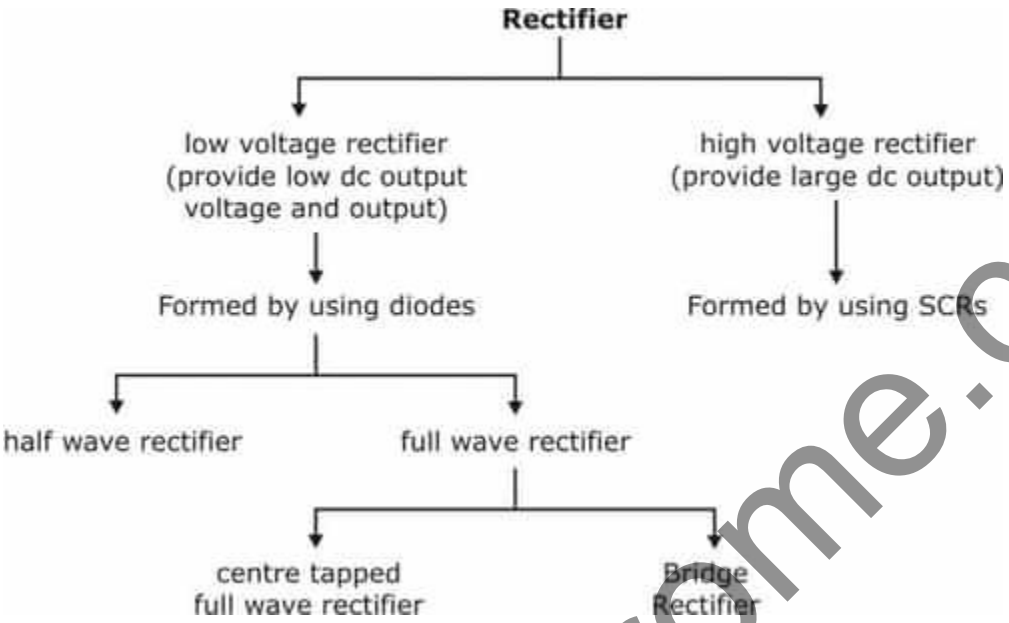
Figure 8

Drawbacks of Zener Voltage Regulators

- The Zener diode can be operated as a voltage regulator within a limited range of reverse current.
- Power dissipation for the Zener diode is practically large enough to affect the efficiency of the device.

- The output resistance of a Zener voltage regulator is practically not as low as desired for the cascading operation.

Diode Rectifiers



1.1. Half wave Rectifier

Half wave rectifier will rectify only half position of input either positive or negative. The basic circuit for half wave rectification is shown in figure 1.

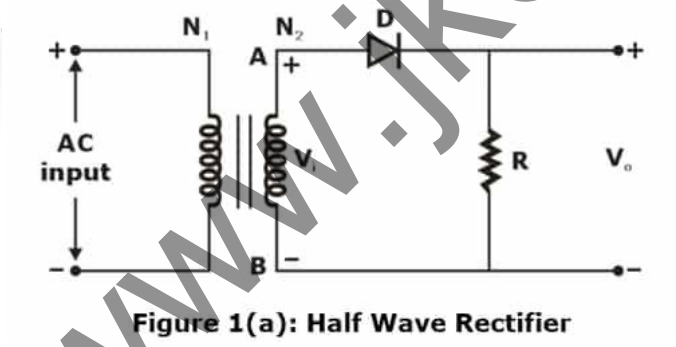


Figure 1(a): Half Wave Rectifier

AC voltage across the secondary winding AB changes polarity after every cycle during the positive half cycle of input ac voltage, end a becomes positive w.r.t end B. This makes the diode forward biased and hence it conducts current.

During the negative half cycle end A is negative w.r.t end B. Under this condition, the diode is reverse biased and it conduct no current.

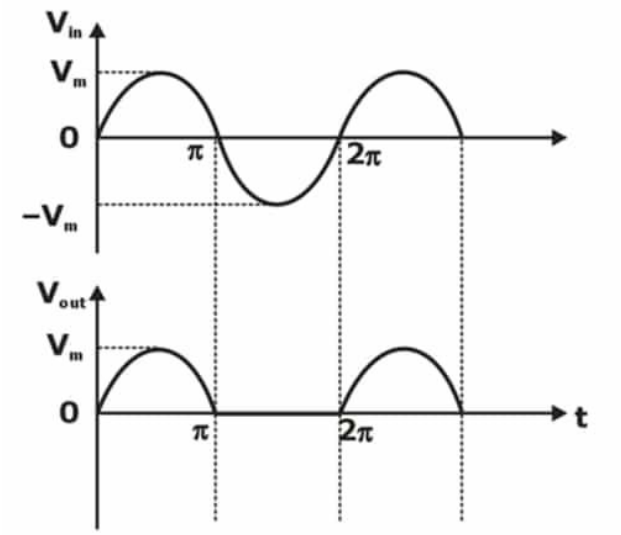


Figure 1 (b): Input and Output waveform

Parameter of output waveform

A. output DC voltage or current

B. output RMS voltage or current

C. Ripple factor

D. Peak inverse voltage

E. Efficiency

A. Output DC voltage or current

$$V_o(DC) = V_o(Avg) = \frac{1}{2\pi}\int_0^{2\pi} V_o(t)\,d\omega t$$

$$= \frac{1}{2\pi}\int_0^{\pi} V_m \sin\omega t\,d\omega t + \frac{1}{2\pi}\int o\ d\omega t$$

$$= \frac{V_m}{2\pi}\left[-\cos\omega t\right]_0^{\pi}$$

$$= \frac{-V_m}{2\pi}\left[\cos\pi - \cos 0\right] = \frac{-V_m}{2\pi}\left[-1-1\right]$$

$$= \frac{-V_m}{2\pi}(-2)$$

$$\boxed{V_o(DC) = \frac{V_m}{\pi}}$$

or $\boxed{V_o(DC) = 0.318\,V_m}$

$$I_o(DC) = \frac{V_o(DC)}{R} = \frac{V_m}{R\pi} = \frac{I_m}{\pi}$$

$$\boxed{I_o(DC) = \frac{I_m}{\pi} = 0.318\,I_m}$$

B. Output RMS voltage or current

$$V_o(rms) = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} V_0^2(t)\, d\omega t}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{\pi} (V_m \sin\omega t)^2\, d\omega t + \frac{1}{2\pi}\int_{\pi}^{2\pi} o\, d\omega t}$$

$$= \sqrt{\frac{V_m^2}{2\pi}\int_0^{\pi} \frac{1-\cos 2\omega t}{2} d\omega t}$$

$$= \sqrt{\frac{V_m^2}{4\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_0^{\pi}}$$

$$= \sqrt{\frac{V_m^2}{4\pi}\left[(\pi - 0) - \frac{1}{2}(\sin 2\pi - \sin 0)\right]}$$

$$= \sqrt{\frac{V_m^2}{4\pi}\left[\pi - \frac{1}{2}(0-0)\right]}$$

$$= \sqrt{\frac{V_m^2}{4\pi} \times \pi} = \sqrt{\frac{V_m^2}{4}}$$

$$= \frac{V_m}{2}$$

$$\therefore \boxed{V_o(rms) = \frac{V_m}{2}}$$

$$I_o(rms) = \frac{V_o(rms)}{R} = \frac{V_m}{R \cdot 2} = \frac{I_m}{2}$$

$$\boxed{I_o(rms) = \frac{I_m}{2}}$$

$$\boxed{I_m = \frac{V_m}{R}}$$

C. Ripple factor

A measure of the fluctuating components is given by the ripple factor which is defined as

$$\gamma = \frac{\text{rms value of alternating components of wave}}{\text{Average value of wave}}$$

$$\boxed{\gamma = \sqrt{\left(\frac{V_o\,(rms)}{V_o\,(DC)}\right)^2 - 1} = \sqrt{\left[\frac{I_o\,(rms)}{I_o\,(DC)}\right]^2 - 1}}$$

Which is sometime approximated as,

$$= \frac{V_o\,(rms)}{V_o\,(DC)} \text{ or } \frac{I_o\,(rms)}{I_o\,(DC)}$$

$$= \frac{V_{ac}}{V_{dc}} \text{ or } \frac{I_{ac}}{I_{dc}}$$

Ripple factor of half wave rectifier

$$\gamma = \sqrt{\left(\frac{V_m/2}{V_m/\pi}\right)^2 - 1}$$

$$= \sqrt{\frac{\pi^2}{4} - 1}$$

$$\boxed{\gamma = 1.21}$$

$$\boxed{\gamma(\%) = 121\%}$$

D. Peak inverse voltage (PIV)

The maximum reverse voltage the diode can with stand without breakdown.

$$\boxed{PIV = V_m}$$

E. Current handling capability of a diode

It is maximum current, that should not exceed otherwise breakdown occurs.

F. Efficiency

It is a measure of the ability of a rectifier to convert AC power into dc power.

$$\boxed{\eta = \frac{P_o\,(dc)}{P_{in}\,(ac)} \times 100}$$

$$= \frac{\text{output dc power}}{\text{input ac power}} \times 100$$

$P_o\,(DC) = V.I = V_o(DC) \cdot I_o(DC)$

$P_{in}\,(AC) = V_{rms} \cdot I_{rms}$

$$\eta = \frac{V_o\,(DC) \cdot I_o\,(DC)}{V_{rms} \cdot I_{rms}} \times 100$$

$$= \frac{V_m / \pi \cdot I_m / \pi}{V_m / 2 \cdot I_m / \pi} \times 100$$

$$\eta = \frac{4}{\pi^2} \times 100$$

$= 0.405 \times 100$

$\boxed{\eta = 40.5\%}$

Conclusion

- It rectifies one half of the input AC signal
- $V_o\,(dc) = \frac{V_m}{\pi} = 0.318\,V_m$
- $I_o\,(dc) = \frac{I_m}{\pi} = 0.318\,I_m$
- $V_o\,(rms) = \frac{V_m}{2}$
- $I_o\,(rms) = \frac{I_m}{2}$
- $I_m = \frac{V_m}{R}$
- $\gamma = 1.21$
- PIV = V_m
- Time period = T = 2π

Disadvantage of half wave rectifier

(i) $V_o\,(DC) = 0.318\,V_m$

Output DC voltage is only 31.8% of peak input voltage V_m

(ii) η = 40.5%

Efficiency is only 40.5%, that is only 40.5% is converted into DC remaining will be lost.

1.2. Full Wave Rectifier

In full wave rectification, current flows through the load in the same direction for both half cycles of input ac voltage. This can be achieved with two diodes working alternatively. For the positive half cycle of input voltage, one diode supplies current to load and for the negative half cycle, the other diode does so; current being always in the same direction through the load.

The following two circuits are used for full wave rectifier

(a) Centre- tap full wave rectifier

(b) Full wave bridge rectifier

1.2.1 Centre-Tapped Full-wave Rectifier

The circuit of a centre-tapped full-wave rectifier is shown in Figure 2(a). This circuit is seen to comprise two half-wave circuits which are so connected that conduction takes places through one diode during one half of the power cycle and through other diode during the second half of the power cycle.

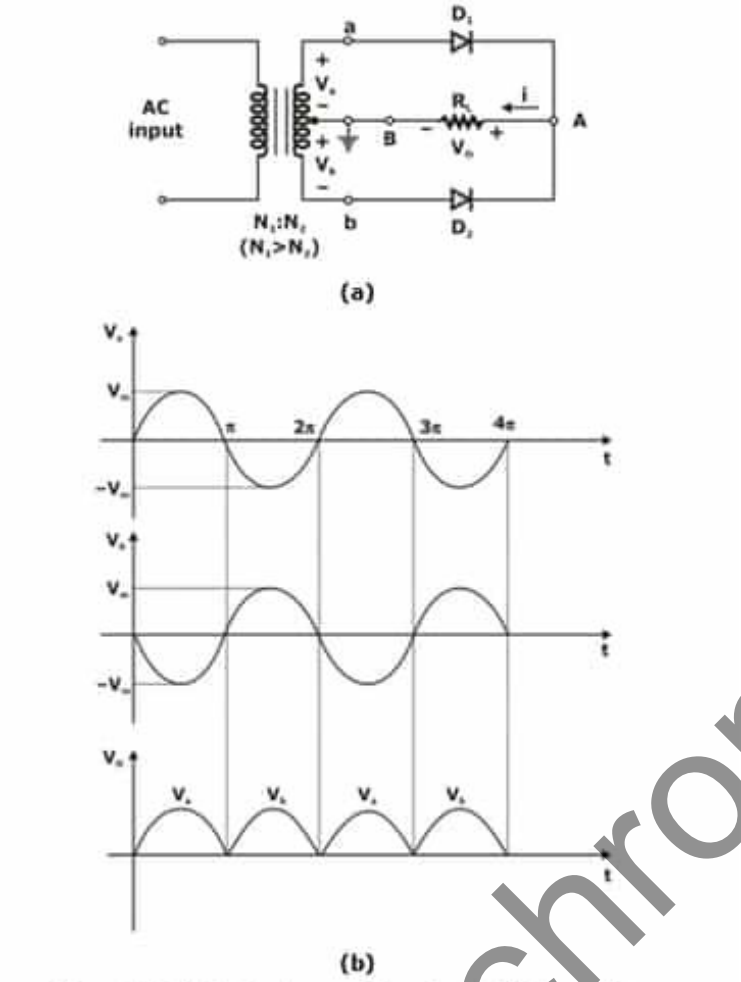


Figure 2: (a) Centre tap rectifier circuit, (b) waveform

In this rectifier center-tapped step down transformer has been used, in which secondary winding is divided into two halves, each half having equal number of turns. In $N_1 : N_2$ center-tapped transformer, primary winding has N_1 turns and each half of secondary winding has N_2 turns.

When center terminal of secondary winding is grounded, voltage at nodes a and b will have equal magnitude but opposite sign;

i.e., $V_b = - V_a$

if $V_a = V_m \sin\alpha$

then $V_b = - V_m \sin\alpha$

Operation

- When $0 < \alpha < \pi$

Then V_a is positive so diode D_1 is forward biased and in this case V_b is negative so diode D_2 is reverse biased. As diode D_1 is in conduction mode so node 'a' gets shorted to R_L therefore Vo= Va

- When $\pi < \alpha < 2\pi$

Then V_a is negative so diode D_1 is reverse biased and V_b is positive so diode D_2 is forward biased. As diode D_2 is in conduction mode so node 'b' gets shorted to R_L therefore Vo= Vb

Parameter of full wave rectifier

A. output DC component

B. output RMS value

C. Ripple factor

D. Peak Inverse voltage

E. Efficiency

A. Output DC voltage

$$V_o(DC) = V_o(Avg) = \frac{1}{T/2}\int_0^{T/2} V_o(t)\,dt$$

$$= \frac{2}{T}\int_0^{T/2} V_m \sin\omega t\,dt$$

$$= \frac{2V_m}{T}\left[\frac{-\cos\omega t}{\omega}\right]_0^{T/2}$$

$$= \frac{2V_m}{T}\left[\frac{-\cos\frac{2\pi}{T}\cdot\frac{T}{2} + \cos 0}{2\pi/T}\right]$$

$$= \frac{V_m}{\pi}\left[-\cos\pi + \cos 0\right]$$

$$= \frac{2V_m}{\pi}$$

$$\boxed{V_o(DC) = \frac{2V_m}{\pi} = 0.636V_m}$$

$$I_o(DC) = \frac{V_o(DC)}{R_L} = \frac{2V_m}{R_L\pi} = \frac{2I_m}{\pi}$$

$$\boxed{I_o(DC) = \frac{2I_m}{\pi} = 0.636\, I_m}$$

B. Output RMS value

$$V_o(rms) = \sqrt{\frac{1}{T/2}\int_0^{T/2} V_0^2(t)\,dt}$$

$$= \sqrt{\frac{2V_m^2}{T}\int_0^{T/2} \sin^2 \omega t\, dt}$$

$$= \sqrt{\frac{2V_m^2}{T}\int_0^{T/2} \frac{(1-\cos 2\omega t)}{2} dt}$$

$$= \sqrt{\frac{2V_m^2}{T}\frac{1}{2}\left[t - \frac{\sin 2\omega t}{2\omega}\right]_0^{T/2}}$$

$$= \sqrt{\frac{V_m^2}{T \times 2 \times 2\frac{\pi}{T}}\left[\left(\frac{T}{2} - 0\right)2 \times \frac{2\pi}{T} - (\sin 2\pi - \sin 0)\right]}$$

$$= \sqrt{\frac{V_m^2}{4\pi}[2\pi - 0]}$$

$$= \sqrt{\frac{V_m^2}{2}}$$

$$\boxed{V_o(rms) = \frac{V_m}{\sqrt{2}}}$$

Similarly, $\boxed{I_o(rms) = \frac{I_m}{\sqrt{2}}}$

3. Ripple factor

$$\gamma = \sqrt{\left(\frac{I_o(\text{rms})}{I_o(\text{dc})}\right)^2 - 1} \quad \text{or} \quad \sqrt{\left(\frac{V_o(\text{rms})}{V_o(\text{DC})}\right)^2 - 1}$$

$$\gamma = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1}$$

$$\gamma = \sqrt{\frac{\pi^2}{8} - 1}$$

$$\boxed{\gamma = 0.483}$$

$$\boxed{\gamma(\%) = 48.3\%}$$

4. Efficiency

$$\eta = \frac{\text{output DC power}}{\text{input AC power}} \times 100$$

$$= \frac{V_o(\text{DC})I_o(\text{DC})}{V_{rms}I_{rms}} \times 100$$

$$= \frac{2V_m/\pi \;\; 2I_m/\pi}{V_m/\sqrt{2} \;\; I_m/\sqrt{2}} \times 100$$

$$= \frac{4\times 2}{\pi^2} = \frac{8}{\pi^2} \times 100 = 0.81 \times 100$$

$$\boxed{\eta = 81\%}$$

5. Peak inverse voltage

$$\boxed{PIV = 2V_m}$$

Conclusion

- $V_o\,(DC) = \frac{2V_m}{\pi} = 0.636V_m$
- $I_o\,(DC) = \frac{2I_m}{\pi} = 0.636\,I_m$
- $\gamma = 0.483$
- $\eta = 81\%$
- $V_{rms} = \frac{V_m}{\sqrt{2}}$
- $I_{rms} = \frac{V_m}{\sqrt{2}}$
- Time period, T = T/2 = π

1.2.2. Bridge Rectifier

The full wave rectifier circuit requires a center-tapped transformer where only one half of the total ac voltage of the transformer secondary winding is utilized to convert into dc output. Now consider a different configuration of full wave rectifier circuit, called bridge rectifier, where entire AC voltage of the transformer secondary is used to convert into DC voltage.

Figure 3 shows a bridge rectifier circuit. There are four diodes D_1, D_2, D_3 and D_4 which form the four arms of the bridge. AC from transformer secondary is fed to two corners and the load resistance R_L is connected to other two corners.

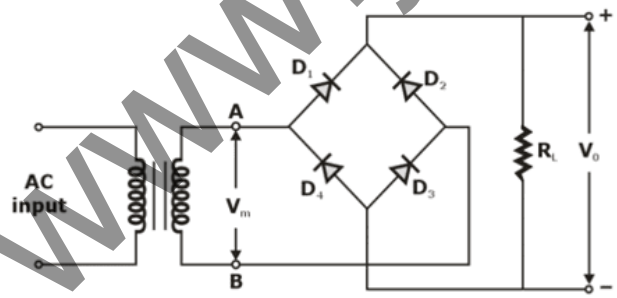


Figure 3: Bride Rectifier

During positive half-cycle of input, point A is positive, diodes D_1 and D_3 are forward biased and diodes D_2, D_4 are reverse biased then, the current flows through diodes D_1, the load R_L and through diode D_3 back to the negative polarity

of the transformer secondary. During negative half cycle of input point B is more positive than point A, thus diode D_2, D_4 are forward biased and diode D_1 and D_3 are reversed biased, then the direction of current flow will be through diode D_2 load R_L and diode D_4. In both case the current flowing through resistor R_L is in same direction, thus it is unidirectional current and we obtain full wave rectification.

BJT & FET: Biasing & Operation

Junction Transistor

- Both the electrons and holes take part in the conduction process for bipolar devices.
- BJT consists of two p-n junctions manufactured in a special way and connected in series, back to back.
- The transistor is generally a 3-terminal device with emitter, base and collector terminals.
- From the physical structure, BJTs can be divided into 2 groups: NPN and PNP transistors.

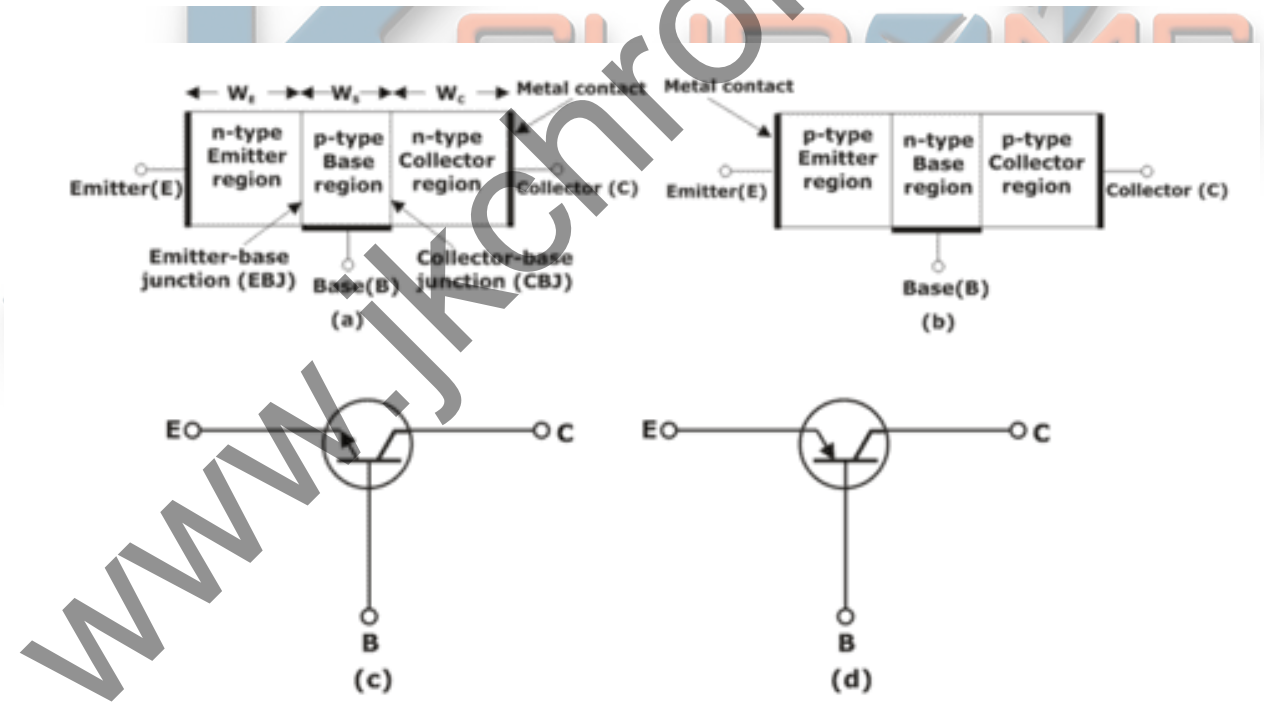


Figure: Simplified block diagram of (a) n-p-n (b) p-n-p and **circuit symbol** of (c) n-p-n and (d) p-n-p bipolar transistors

- **Modes of operation:**

The transistor consists of two p-n junctions, the emitter-base junction (EBJ) and the collector-base junction (CBJ). Depending on the bias condition (forward or reverse) of each of these junctions, different modes of operation of BJT are obtained, as shown in below table.

S. No.	Mode	EBJ	CBJ	Properties	Applications
1.	Cut-off	Reverse bias	Reverse bias	Very high internal resistance	OFF switch
2.	Active	Forward bias	Reverse bias	Excellent transistor action	Amplifier
3.	Saturation	Forward bias	Forward bias	Very low internal resistance	ON switch
4.	Reverse active	Reverse bias	Forward bias	Very poor transistor action	Attenuator (Practically not used)

Table-1: BJT modes of operation

- **Active Mode:**

When the emitter-base junction of the transistor is forward biased and the collector-base junction is reverse biased, the transistor operates in active region. In this mode transistor is used as amplifier. This bias configuration is shown in below figure for n-p-n and p-n-p transistors.

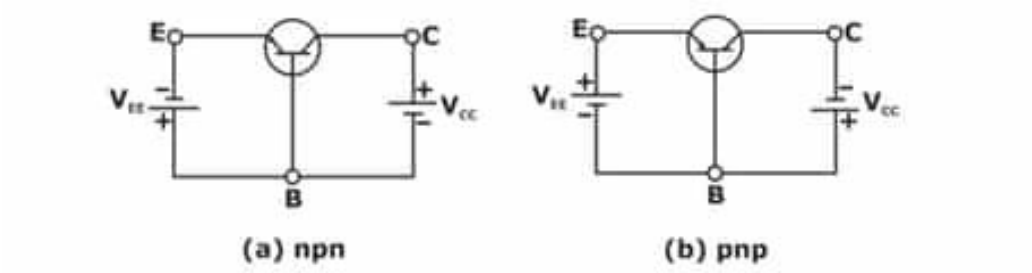


Figure: Transistors Biased in forward Active mode (a) n-p-n (b) p-n-p

- **Saturation Region**

When both the emitter-base junction and collector-base junction are forward biased, the transistor operates in saturation region. Transistor has a large current in saturation mode. In the saturation mode , the transistor is used as closed switch.

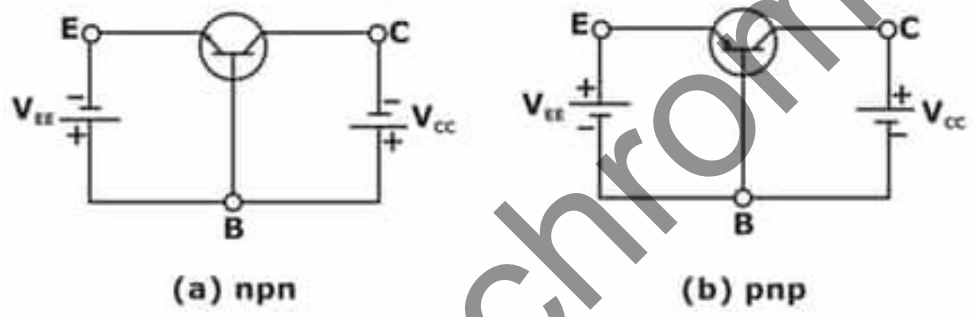


Figure: Transistor Biased in saturation mode (a) n-p-n (b) p-n-p

- **Cut-off region**

When both the emitter-base and collector-base junctions are reverse biased, transistor operates in cut-off region. In cut-off mode the current through the transistor is zero(ideally). In this case the transistor is operated as an open switch. Both n-p-n and p-n-p transistor are biased in cut-off mode as shown in below figure.

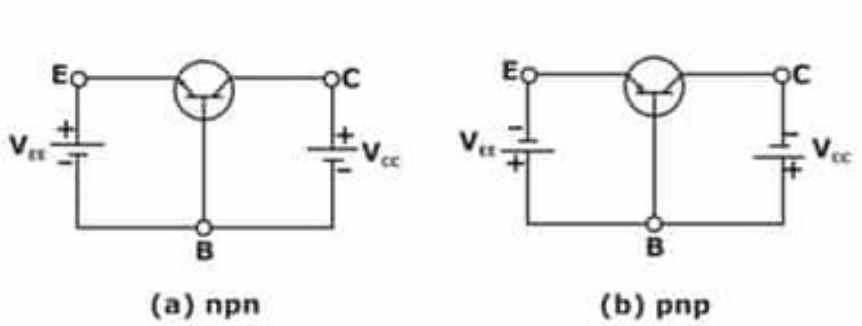


Figure: Transistor Biased in cut off mode (a) n-p-n (b) p-n-p

- **Reverse Active Region or Inverse Region**

When the emitter-base junction of the transistor is reverse biased and the collector-base junction is forward biased, the transistor is said to be in reverse active mode. This mode of operation is not often used. In below figure, transistors are biased in reverse active mode.

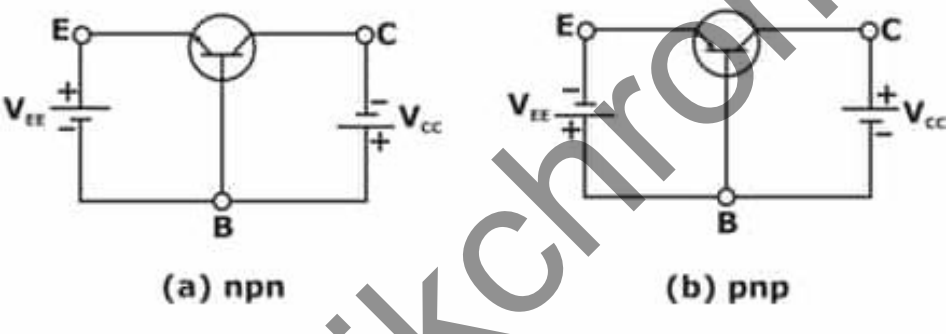


Figure: Transistor Biased in Reverse Active Mode (a) n-p-n (b) p-n-p

4. Current Relationship in BJT

If Bipolar transistor is treated as single node, then by Kirchhoff's current law

$$I_E = I_C + I_B$$

This relation is applicable in all three configurations of BJT.

Relation between current gain

For dc mode, common emitter current gain

$$\beta = \frac{I_C}{I_B}$$

And common base current gain

$$\alpha = \frac{I_C}{I_E}$$

Applying these expressions in above equation,

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

$$\therefore \alpha = \frac{\beta}{\beta + 1}$$

$$\text{or } \beta = \frac{\alpha}{1 - \alpha}$$

Relation between leakage current

For common emitter configuration,

$$I_C = \alpha I_E + I_{CBO}$$

$$\Rightarrow I_C = \alpha (I_C + I_B) + I_{CBO} \qquad (I_E = I_C + I_B)$$

$$\Rightarrow (1 - \alpha) I_C = \alpha I_B + I_{CBO}$$

$$\Rightarrow I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{1}{1 - \alpha} I_{CBO}$$

$$= \beta I_B + \frac{1}{1 - \alpha} I_{CBO}$$

Since the current equation for the common base configuration is as

$$I_C = \beta I_B + I_{CEO}$$

Comparing above both equations,

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$$

$$\text{or } I_{CEO} = (1 + \beta) I_{CBO}$$

Transistor Configuration

The transistors can be connected in the following three different configurations, Depending upon the terminals which are used as a common terminal to the input and output terminals.

- Common Base Configuration
- Common Emitter Configuration
- Common Collector Configuration

a) Common Base Configuration

- In this configuration base terminal is connected to a common terminal.
- The input signal is applied between the emitter and base terminals.
- The output signal is taken between the collector and base terminals.

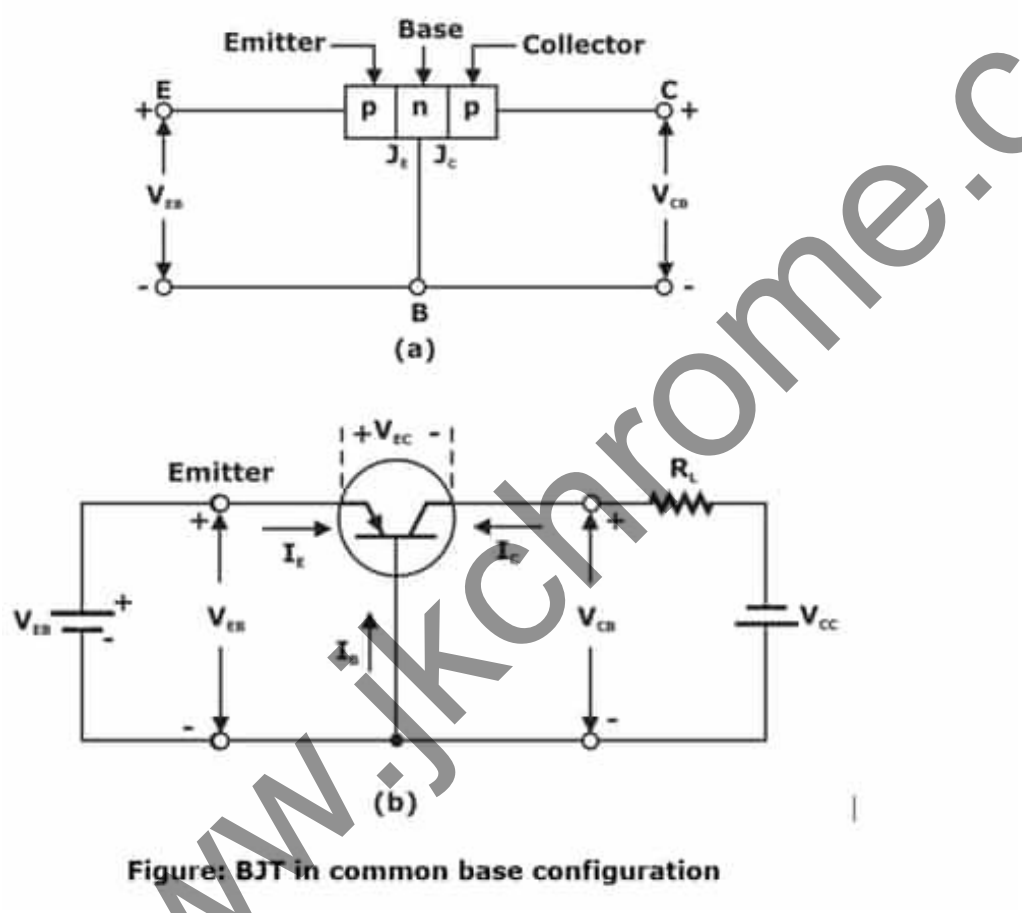


Figure: BJT in common base configuration

Properties of CB configuration

- Lowest input resistance (R_i < 100 Ω)
- Highest output resistance (R_0 > 1 Ω)
- Lowest current gain (α < 1)
- Highest voltage gain
- Medium power gain (Typical value 68)
- Output and input voltages are in phase i.e. phase shift is 0°.

- In CB amplifier current gain is less and therefore bandwidth is large and hence CB amplifier is widely used as high frequency amplifier.

Applications

- As a non-inverting voltage amplifier
- As a high frequency amplifier
- As an impedance matching device between low resistance to high resistances.

b) Common Emitter Configuration

- In this configuration, emitter terminal is connected to a common terminal
- The input signal is applied between the emitter and base terminals.
- The output signal is taken between the collector and base terminals

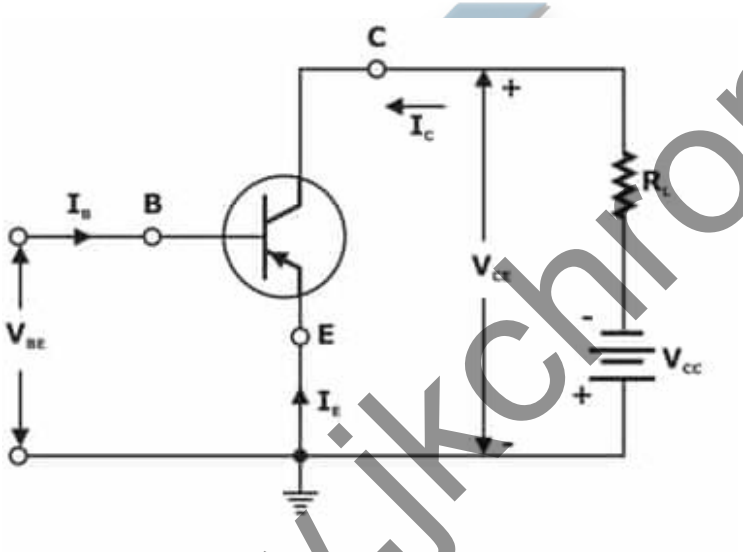


Figure: Common-Emitter Configuration.

Properties

- Moderate input resistance (around 1 kΩ).
- Moderate output resistance (50 kΩ to 500 kΩ).
- Moderate current gain (Typical value 49).
- Moderate voltage gain.
- Highest power gain (Typical value 4226).
- Output and input voltages are out of phase i.e. phase shift = 180°.

Application

It is the most common and frequently used amplifier circuit.

c) Common Collector Configuration

- In this configuration, collector terminal is connected to a common terminal.
- The input is applied between the base and collector terminals.
- The output is taken between the emitter and collector terminals.

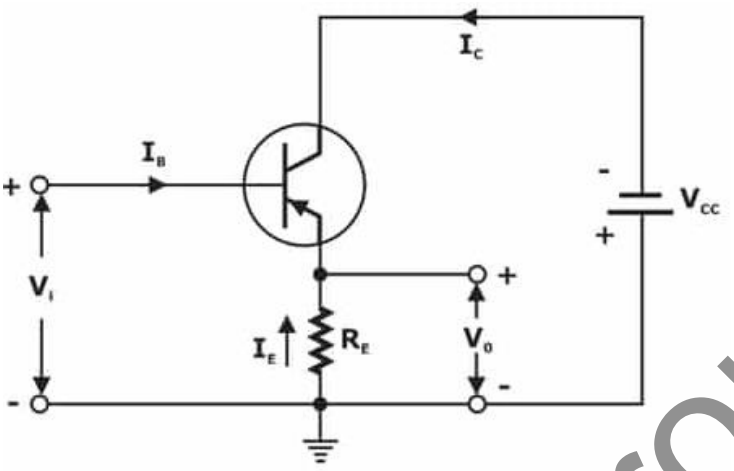


Figure: Common Collector Configuration

Properties

- Highest input resistance (50 kΩ to 500 kΩ).
- Lowest output resistance (< 100 Ω).
- Highest current gain.
- Lowest voltage gain.
- Voltage gain is less than 1 or very close to 1.
- Lowest power gain (Typical value 48).
- Output and input voltages are in phase i.e. phase shift is 0°.
- Common collector configuration is also known as emitter follower.
- Emitter follower is basically a Current Controlled Voltage Source (CCVS).

Applications

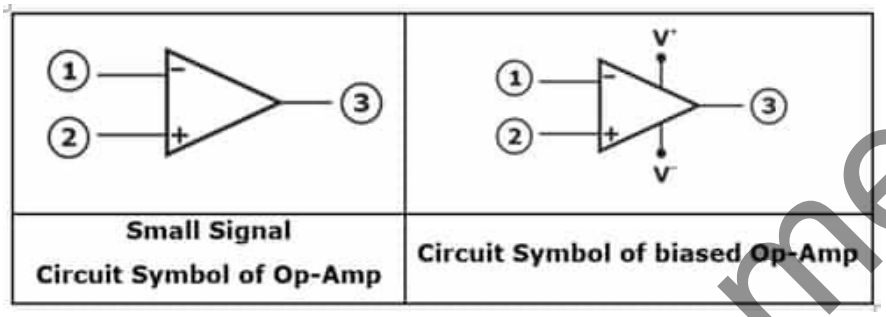
- As an audio frequency power amplifier.
- As a butter (impedance matching device between high resistance to low resistance).
- In designing of voltage sweep circuits.
- As a high input resistance device.

- As a “Boot strap emitter follower”.

Operational Amplifiers

1. Introduction

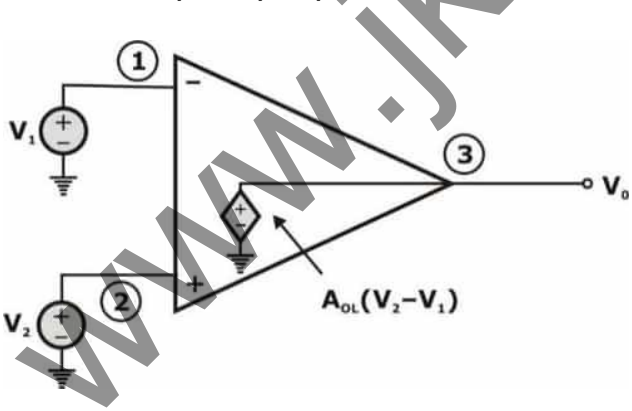
An operational amplifier (Op-Amp) is an integrated circuit that amplifies the difference between two input voltages and produces a single output. From signal point of view, the Op-Amp has two input terminals and one output terminal as shown in figure below.



2. Characteristics of Ideal Op-Amp:

The ideal Op-Amp senses the difference between two input signals and amplifies this difference to produce an output signal. The output terminal voltage is the voltage at the output terminal measured with respect to ground.

The ideal Op Amp equivalent is shown in figure below.

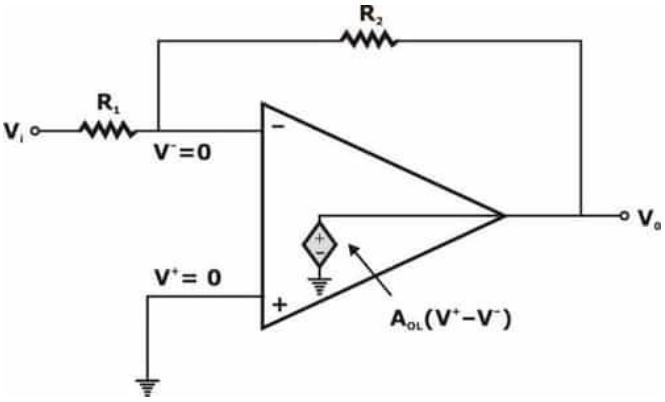


Here,

A_{OL} = open loop gain

1. It has infinite input impedance and zero output impedance.

2. The common mode gain is zero (or) equivalently, common mode rejection ratio is infinite.
3. The open loop gain of ideal op-amp is infinite
4. The ideal op-amp has infinite bandwidth and infinite slew-rate.
5. We stated that if the open loop gain (A_{OL}) is very high, then the two input V_1 and V_2 must be nearly equal. Since, if V_2 is at ground potential, voltage V_1 must also be approximately zero volts as shown below.



3. Feedback in Op Amp:

3.1. Negative Feedback:

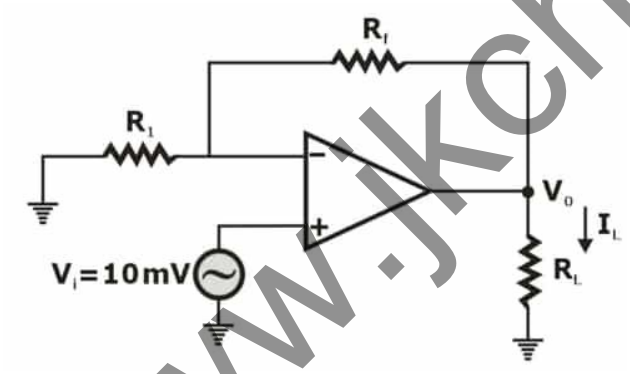


Figure: Non-Inverting Amplifier

Here, Closed loop gain $= \boxed{A_{CL} = 1 + \frac{R_f}{R_1}}$

Conclusion: When the Op-Amp relates to negative feedback, the voltage gain will reduce.

i.e. $$A_{CL} = \frac{A_d}{1 + A_d\beta}.$$

So, for any input V_i in the range of "mV" or 0V, output V_0 will be very close to 0.

3.2. Positive Feedback:

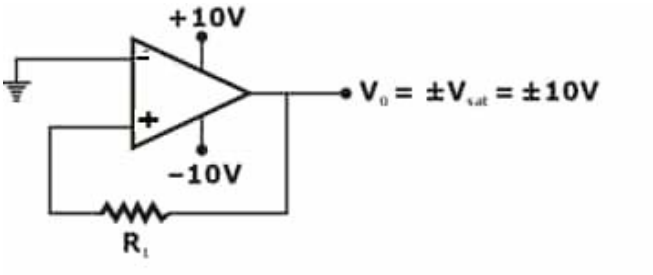


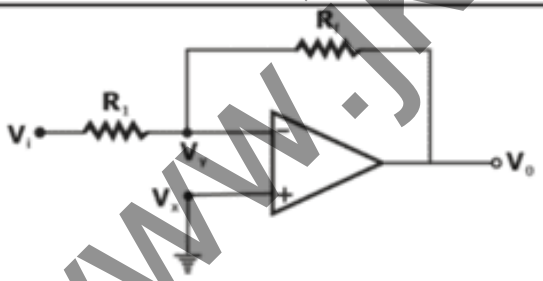
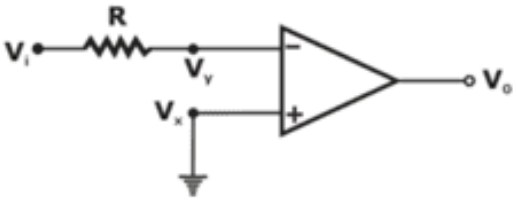
Figure: Positive Feedback Amplifier

Note: Multivibrator works in open or closed loop of positive feedback.

4. Virtual-Ground and Comparator:

- Virtual ground theory is applicable only in "Negative feedback". It is not applicable in positive feedback and open loop.
- Comparator theory is applicable for open loop and positive feedback.

Table: Comparison between Negative feedback and Open-loop

Negative feedback [Virtual ground]	Open-loop [Comparator]
	
Here, $V_y = V_x$ $V_y \neq V_i$	Here, $V_y = V_i$ $V_y \neq V_x$

5. Slew-Rate:

Slew rate is defined as the maximum rate at which amplifier output can change. It is expressed in Volts per microsecond (V/μs) i.e.

$$SR = \frac{\Delta V_o}{\Delta t} V/\mu s$$

Here, ΔV_0 = Small change in output voltage in a small interval Δt.

In terms of input voltage, slew rate can be expressed as:

$$SR = A_{CL} \frac{\Delta V_i}{\Delta t}$$

Here, A_{CL} = closed loop gain,

ΔV_i = Small change in input voltage in a small interval Δt

6. Differential and Common Mode operation:

6.1. Differential Inputs:

When separate inputs are applied to the op-Amp, the resulting difference signal is the difference between the two inputs

i.e.

$V_d = V_{i1} - V_{i2}$

Here, V_{i1}, V_{i2} = inputs to the op-Amp.

6.2. Common Inputs:

If there is no difference between the input signals, a common signal element due to the two input signals can be defined as the average of the sum of the two signals.

$$V_c = \frac{1}{2}(V_{i1} + V_{i2})$$

Here, V_{i1}, V_{i2} are the inputs to the Op-Amp.

6.3. Output-Voltage:

Since, any signal applied to an Op-Amp is generally have both in phase and out of phase components, the resulting output can be expressed as:

$V_0 = A_dV_d + A_cV_c$

Here,

A_d = differential voltage

V_c = Common voltage

A_d = Differential gain of the amplifier

A_c = common mode gain of the amplifier

6.4. Common Mode Rejection Ratio: (CMRR)

CMRR is defined as the ratio of differential voltage gain to the common mode gain.

i.e. $$CMRR = \frac{A_d}{A_c}$$

In decibels, we may express

$$CMRR(dB) = 20\log_{10}\left[\frac{A_d}{A_c}\right]$$

7. Applications of Operational amplifiers

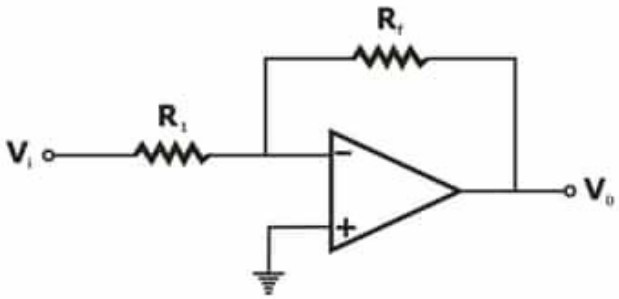
- Inverting Amplifier
- Non-inverting Amplifier
- Differentiator
- Differential Amplifier
- Voltage follower
- Selective inversion circuit
- Current-to-voltage converter
- Active rectifier
- Integrator
- Comparator
- Filters
- Voltage comparator
- Signal Amplifier

7.1. Inverting-Amplifier:

The voltage gain for the inverting Amplifier is given by:

$$A_v = \frac{-R_f}{R_1}$$

Below figure shows the inverting amplifier.



7.2. Non-Inverting Amplifier

The voltage gain for the non-inverting amplifier is given by:

$$A_V = \frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

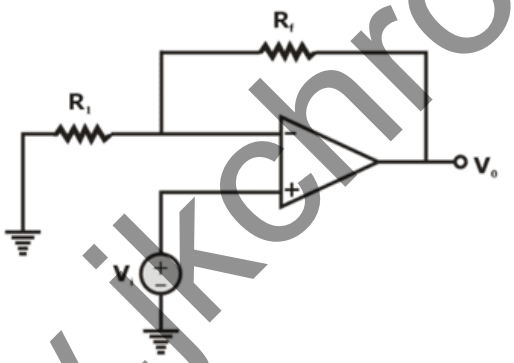
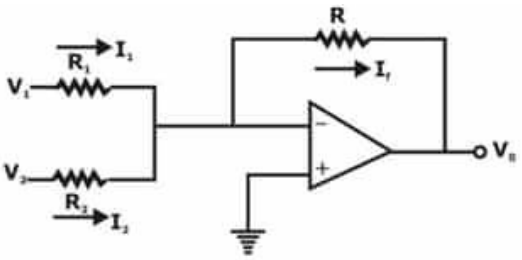


Figure: Non-Inverting Amplifier

7.3. Voltage Adder:

7.3.1. Inverting Adder:



$I = I_f$

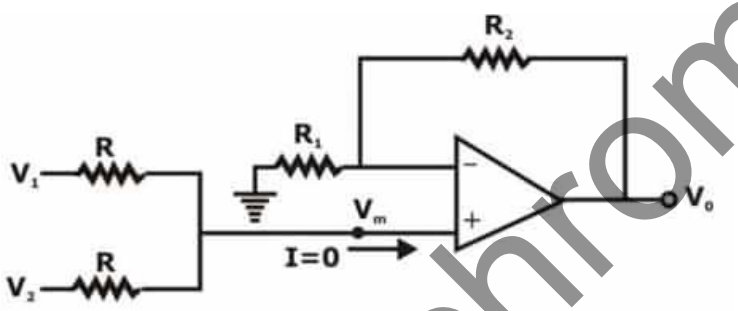
$I_1 + I_2 = I_f$

$$\frac{V_1}{R} + \frac{V_2}{R} = \frac{0 - V_0}{R}$$

$$-(V_1 + V_2) = V_0$$

$$\therefore \quad \boxed{V_0 = -(V_1 + V_2)}$$

7.3.2. Non-Inverting Adder:



$$V_m = \frac{V_1 R}{R_1 + R_2} + \frac{V_2 R}{R_1 + R_2} = \frac{V_1 R}{R + R} + \frac{V_2 R}{R + R}$$

$$V_m = \frac{V_1 + V_2}{2}$$

$$\therefore \quad V_0 = \left(1 + \frac{R_2}{R_1}\right) V_m \quad (\text{if } R_1 = R_2 = R)$$

$$\therefore \quad \boxed{V_0 = (V_1 + V_2)}$$

7.4. Voltage Subtractor Circuit

A Voltage Subtractor circuit consist of an inverting amplifier and a summing amplifier. Output of the inverting amplifier is given by:

$$V_3 = \frac{-R_f}{R_1} V_1$$

So, the output voltage of the summing amplifier is obtained as:

$$V_0 = -\left[\frac{R_f}{R_3} V_3 + \frac{R_f}{R_2} V_2\right]$$

$$= -\left[\frac{R_f}{R_3}\left(-\frac{R_f}{R_1} V_1\right) + \frac{R_f}{R_2} V_2\right]$$

$$\text{Thus, } V_0 = \frac{R_f^2}{R_1 R_3} V_1 - \frac{R_f}{R_2} V_2$$

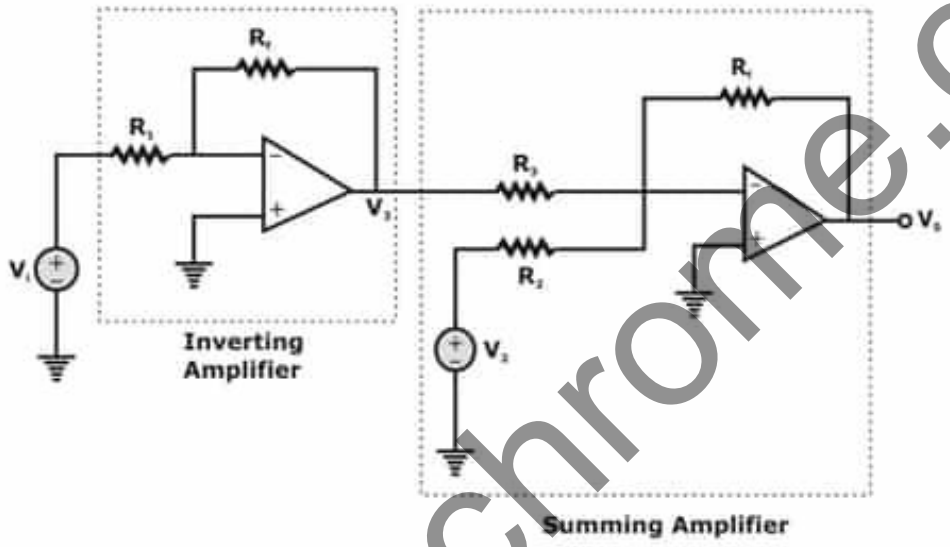
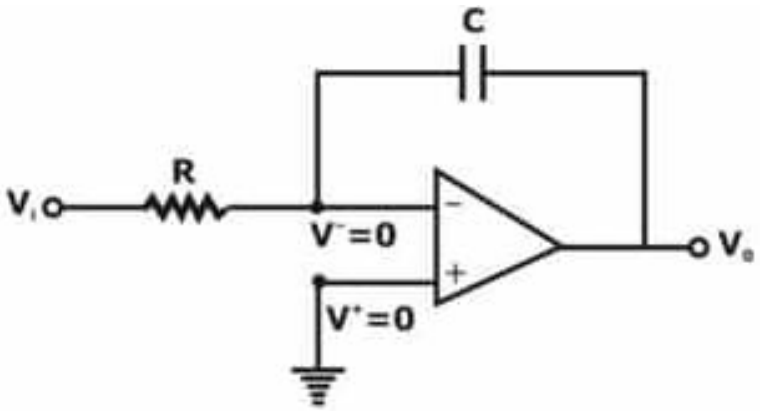


Figure: Voltage Subtractor Circuit

7.7. Integrator circuit:



Applying KCL at inverting terminal, we have

$$\frac{0-V_i}{R}+\frac{0-V_0}{1/sC}=0$$

$$\frac{V_0}{V_i}=\frac{-1}{sRC}$$

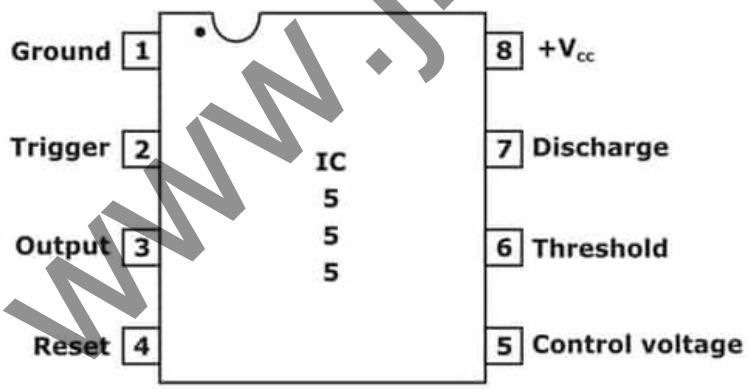
Since, the transfer function shows a pole at the origin, the circuit operates as an integrator (low-pass filter)

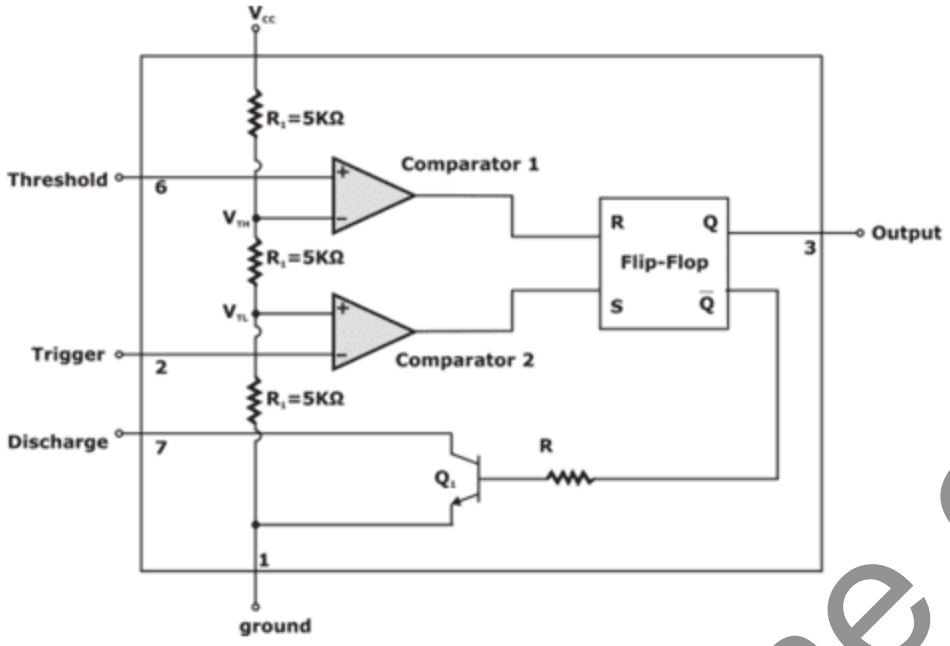
Input-output relation in time domain is —

$$V_0=\frac{-1}{RC}\int V_i dt$$

Timers & Oscillators

1. The 555 Timer Circuit:





Block diagram representation of the internal circuit of the 555-IC timer

A block diagram representation of the 555-timer circuit is shown in figure . The circuit consist of two comparators, an SR flip-flop and a transistor Q_1 that operates as a switch. One power supply V_{CC} is required for operation. A resistive voltage divider, consisting of the three equal valued resistor R_1 which is equal to 5kΩ is connected across V_{CC} and establishes the reference or threshold voltages for the two comparators.

$$V_{TH} = \frac{2}{3}V_{CC} \text{ for comparator 1}$$

And $$V_{TL} = \frac{1}{3}V_{CC} \text{ for comparator 2}$$

SR flip-flop works as a bi-stable circuit having the complementary outputs, denoted as Q and

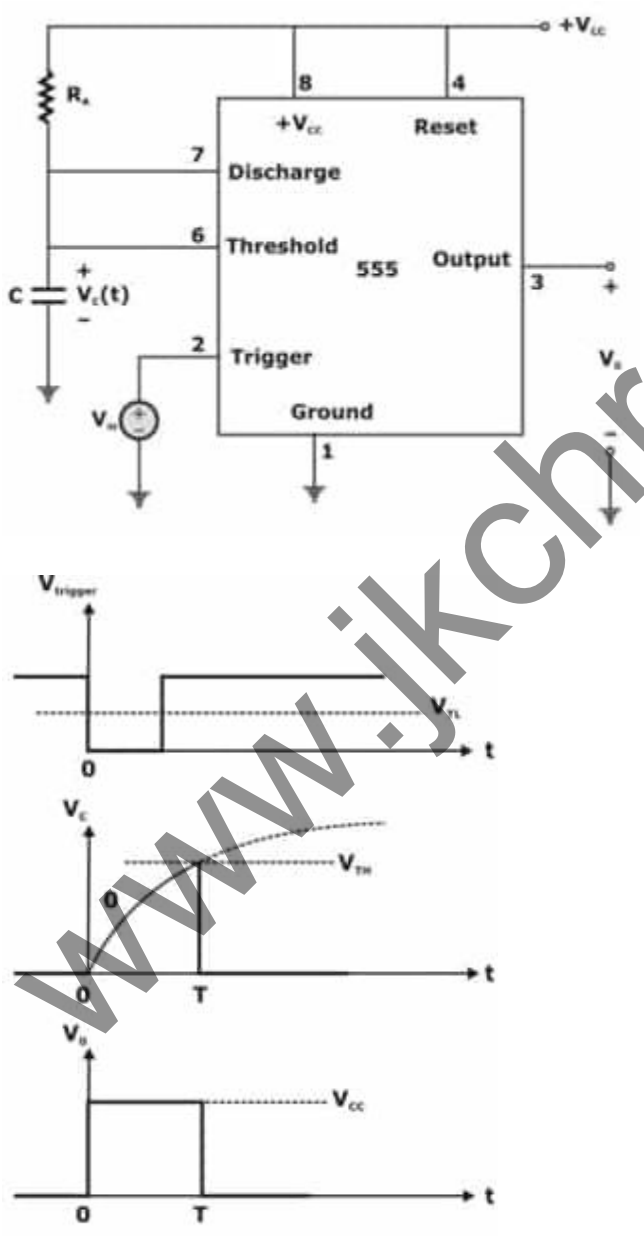
In set state, the output at Q is 'high' (approximately equal to V_{CC}) and that at $\overline{Q}$ is 'low' (approximately equal to 0 V).In reset state, the output Q is low and $\overline{Q}$ is high.

The flipflop is set by applying a high level (V_{CC}) to its set input terminal S and reset by applying to the reset input terminal R. The outputs of comparator 1 and

comparator 2 respectively are connected to the set and reset input terminals of the flip flop.

The positive input terminal of the comparator 1 is connected to a external terminal of the 555 IC is labelled as Threshold. Similarly, the negative input terminal of comparator 2 is connected to an external terminal labelled as Trigger and the collector of transistor Q_1 is connected to a terminal labelled discharge. finally, the output of flip flop Q is connected to output terminal.

2. Implementation of Monostable Multivibrator using 555 Timer:



The external circuitry and waveform of 555 IC as monostable multivibrator is shown in figure 2(a) & (b). Before applications of trigger pulse V_T, The voltage at trigger input is high which is equal to $+V_{CC}$. output and output voltage V_0 is equal to 1. With

$\overline{Q} = 1$

and output voltage V_0 is equal to 1. When

$\overline{Q} = 1$

the discharging transistor Q_1 undergoes to saturation and across the timing capacitor the voltage will be zero i.e., $V_C(t) = 0$.

At t = 0, on the application of trigger V_T (negative going pulse) $<V_{CC}/3$ causes output of comparator C_2 to be high i.e. S = 1. This will set the flip flop with This makes output voltage $V_0 = 0$. Due to

$\overline{Q} = 0.$

the discharge transistor Q_1 will get turned off. After the termination of trigger pulse, the flipflop will remain in

$\overline{Q} = 0.$

state, since S = 0 and R = 0, So no change in state. The timing capacitor charges up exponentially toward final value of V^+ through resistor R.

The capacitor voltage is given by

$$v(t) = V^+(1 - e^{t/RC})$$

.....(i)

When $v(t) = 2/3\ V^+$, the threshold comparator output goes high, resetting the flip flop. Output

then goes high and the output of the 555 goes low. The high output at

$\overline{Q}$

turns on the discharge transistor, allowing the timing capacitor to discharge to near zero volts. The circuit thus returns to its Quiescent state.

The width the output pulse is determined from equ. (i) by putting

$v(t) = 2/3\ v^+$ and $t = T$, then

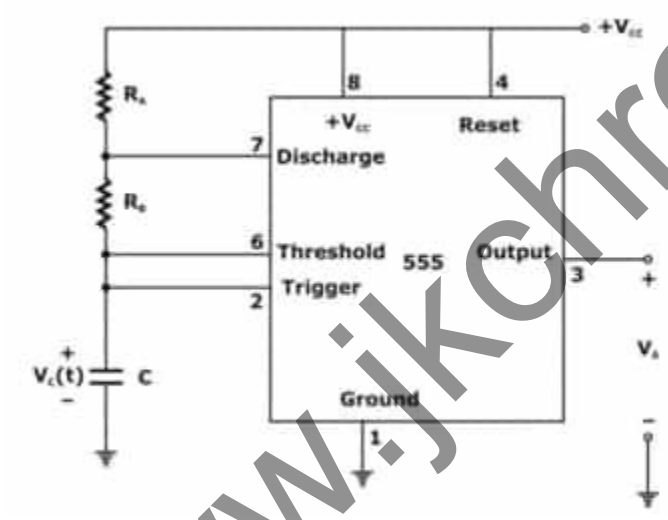
$$\left(\frac{2}{3}\right)V^+ = V^+(1 - e^{T/RC})$$

solving for T,

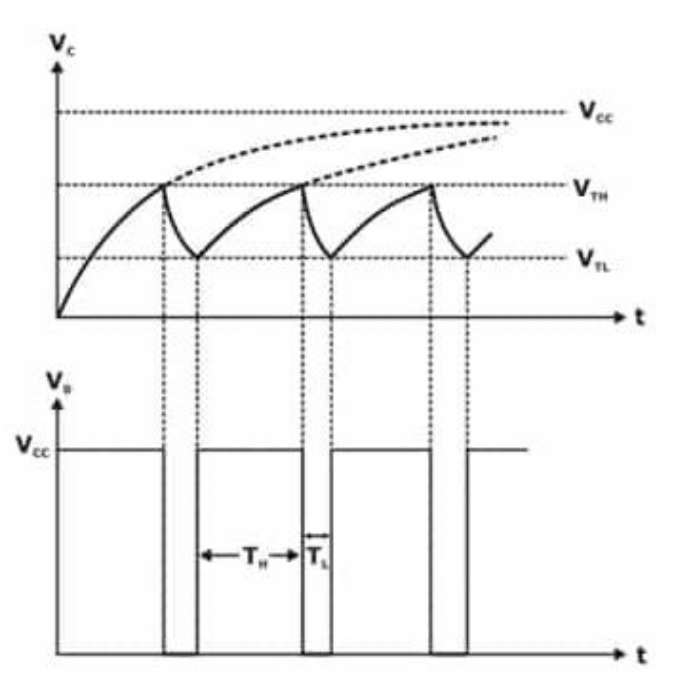
$$\boxed{T = RC \ln (3) = 1.1RC}$$

The width of the output pulse is a function of only the external time constant RC, it is independent of supply voltage V^+ and any internal circuit parameters.

3.Implementation of Astable Multivibrator using 555 Timer:



Astable Multivibrator 555 Circuit



In this the threshold and trigger input is connected together. In astable mode, the timing capacitor C charges through $R_A = R_B$ until v(t) reaches 2/3 V^+. The threshold comparator output then goes high, forcing the flip flop output

to go high. The discharge transistor turns on, and the timing capacitor C discharges through R_B and the discharge transistor.

The capacitor voltage decreases until it reaches (1/3)V^+, at which point the trigger comparator switches stages and sends

$\overline{Q}$

low.

The discharge transistor turns off, and the timing capacitor begins to recharge. When v(t) reaches the threshold level of (2/3) V^+, the cycle repeat itself.

$$V_C(t) = V_{cc} + \left(\frac{V_{cc}}{3} - V_{cc}\right)e^{-t/\tau}$$

$$= V_{cc} - \frac{2V_{cc}}{3}e^{-t/\tau}$$

$$= V_{cc}\left(1 - \frac{2}{3}e^{-t/\tau}\right)$$

At $\tau = T_1$,

$$V_C(t) = \frac{2V_{cc}}{3}$$

$$\frac{2V_{cc}}{3} = V_{cc}\left(1 - \frac{2}{3}e^{-t/\tau}\right)$$

$$\Rightarrow \quad 1 = 2e^{-t/\tau}$$

$$T = \tau \ln 2$$

Therefore, charging time is given as

$$\boxed{T_C = 0.693\,(R_A + R_B)C}$$

When the timing capacitor is discharging, during the time $0 < t' < T_D$, the capacitor voltage is

$$V(t') = \frac{2}{3}V^{+}e^{-t'/\tau_B}$$

Where $\tau_B = R_BC$, at $t' = T_D$, the capacitor voltage reaches the trigger level and

$$V(T_D) = \frac{1}{3}V^{+} = \frac{2}{3}V^{+}e^{-T_D/\tau_B} \quad \text{.....(ii)}$$

solving equation (ii) for the timing capacitor discharge time T_D, yields,

$$\boxed{T_D = \tau_B \ln(2) = 0.693\,R_BC}$$

Total time to given as

$T = T_C + T_D$

$$\boxed{T = 0.693\,(R_A + 2R_B)C}$$

The frequency of oscillation,

$$f = \frac{1}{T} = \frac{1}{T_C + T_D}$$

$$\boxed{f = \frac{1}{0.693(R_A + 2R_B)C} = \frac{1.44}{(R_A + 2R_B)C}}$$

Duty cycle: It is defined as the percentage of time the output is high during one period of oscillation. during the changing time T_C, the output is high and during discharging time T_D, the output is low.

$$\boxed{\text{Duty cycle} = \frac{T_C}{T} \times 100\% = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%}$$

Oscillators

- Oscillators are electronic circuits that generate an output signal without the necessity of an input signal. It produces a periodic waveform on its output with only the DC supply voltage as an input.
- It produces a periodic waveform on its output with only the DC supply voltage as an input.
- Different types of oscillators produce various types of outputs including sine waves, square waves, triangular waves, and sawtooth waves.
- The basic structure of a sinusoidal oscillator consists of an amplifier and a frequency selective network connected in a positive feedback loop as shown in figure 1.

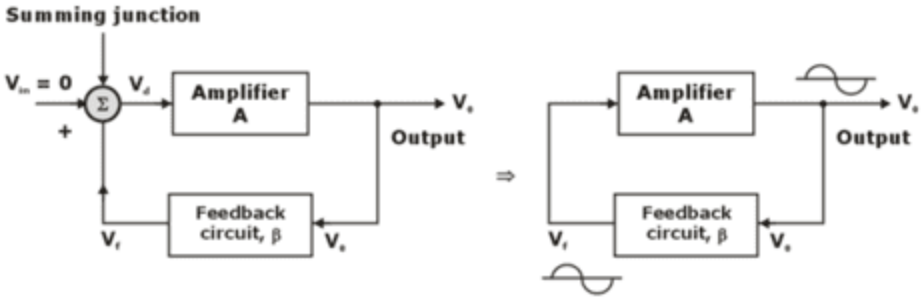


Figure 1: Oscillator Block Diagram

In the block diagram of figure 1,

$V_d = V_f + V_{in}$

$V_0 = AV_d$

$V_f = \beta V_0$

Using these relationships, the following equation is obtained:

$$\frac{V_0}{V_{in}} = \frac{A}{1 - A\beta}$$

However, $V_{in} = 0$ and $V_0 \neq 0$ implies that,

$$A\beta = 1 \quad \ldots\ldots \text{(i)}$$

Expressed in polar form

$$A\beta = 1\angle 0° \text{ or } 360° \quad \ldots\ldots\ldots \text{(ii)}$$

Equation (i) & (ii) gives two requirements for oscillation:

- The magnitude of the loop gain Aβ must be at least 1, and
- The total phase shift of the loop gain Aβ must be equal to 0° or 360°.

The above conditions is known as **Barkhausen** criterion.

In figure 1, if the amplifier causes a phase shift of 180°, the feedback circuit must provide an additional phase shift of 180° so that the total phase shift around the loop is 360°. The type of waveform generated by an oscillator depends on the components in the circuit hence may be sinusoidal, square or triangular. In addition, the frequency of oscillation is determined by the components in the feedback circuit.

Oscillators can be of 2 types:

Feedback Oscillators:

- One type of oscillator is the feedback oscillator, which returns a fraction of the output signal to the input with no net phase shift, resulting in a reinforcement of the output signal.
- After oscillations are started, the loop gain is maintained at 1.0 to maintain oscillations.
- A feedback oscillator consists of an amplifier for gain (either a discrete transistor or an op-amp) and a positive feedback circuit that produces phase shift and provides attenuation.

Relaxation Oscillators:

- Instead of feedback, a relaxation oscillator uses an RC timing circuit to generate a waveform that is generally a square wave or other non sinusoidal waveform.
- Typically, a relaxation oscillator uses a Schmitt trigger or other device that changes states to alternately charge and discharge a capacitor through a resistor.

Oscillation with RC Feedback Circuits

- Three types of feedback oscillators that use RC circuits to produce sinusoidal outputs are the:
  - Wien-bridge oscillator
  - Phase-shift oscillator
  - Twin-T oscillator
- Generally, RC feedback oscillators are used for frequencies up to about 1 MHz.
- The Wien-bridge is by far the most widely used type of RC feedback oscillator for this range of frequencies.
- **Wien Bridge Oscillator**

  Because of its simplicity and stability, one of the most commonly used audio-frequency oscillators is the wein bridge. Figure 2 shows the wein bridge oscillator in which the wein bridge circuit is connected between the amplifier input terminals and the output terminal. The bridge has a series RC network in one arm and a parallel RC network in adjoining arm. In the remaining two arms of the bridge, resistors R_1 and R_2 are connected.

The phase angle criterion for oscillation is that the total phase shift around the circuit must be 0°. This condition occurs only when the bridge is balanced, that is **at resonance.** the frequency of oscillation f_0 is exactly the resonant frequency of the balanced wein bridge and is given by:

$$f_0 = \frac{1}{2\pi RC} = \frac{0.159}{RC}$$

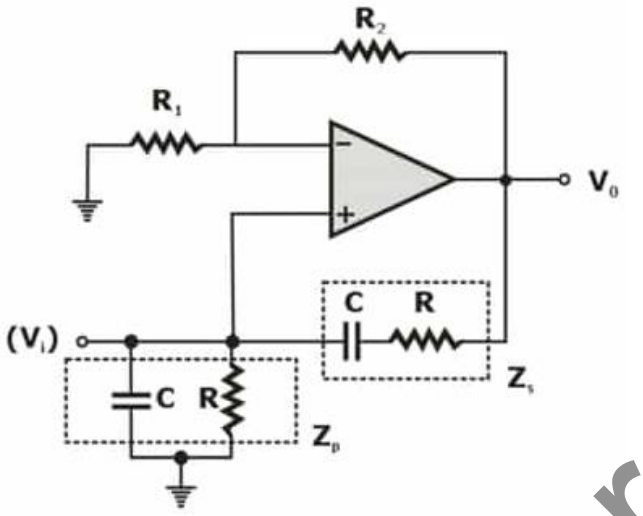


Figure 2: Wein- Bridge Oscillator

Assuming that the resistors are equal in value, and capacitors are equal in value in the reactive leg of the wein bridge. At this frequency the gain required for sustained oscillation is given by

$$A = \frac{1}{\beta} = 3$$

That is $$1 + \frac{R_2}{R_1} = 3$$

or $$\boxed{R_2 = 2R_1}$$

Phase-shift Oscillator

- A phase-shift oscillator relies upon an *R-C* phase shift network to provide the necessary phase relationship between output and input to a CE amplifier. The frequency of oscillation is given by and the phase shift is 180°.

1 Phase-shift Oscillator using Op-Amp:

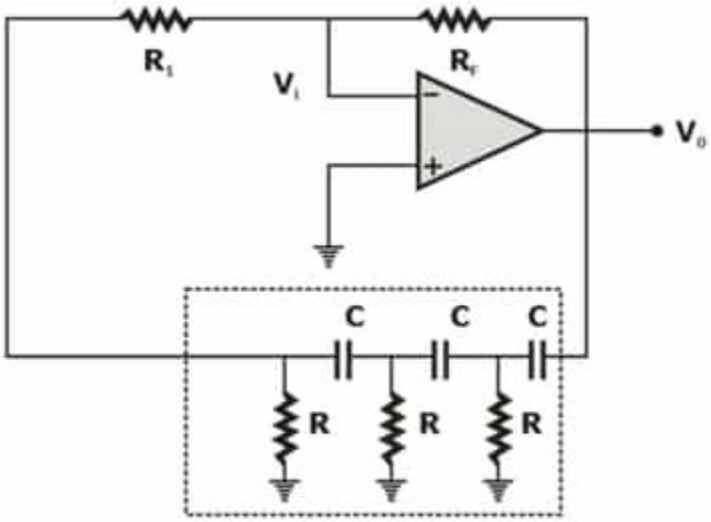


Figure 3: A Phase Shift Oscillator Using Op-amp

The op-amp is used in the inverting mode; therefore, any signal that appears at the inverting terminal is shifted by 180° at the output. An additional 180° phase sift required for oscillation is provided by the cascaded RC networks. Thus, the total phase shift around the loop is 360° (or 0°). At some specific frequency when the phase shift of the cascaded RC networks is exactly 180° and the gain of the amplifier is sufficiently large, the circuit will oscillate at the frequency. This frequency is called the frequency of oscillation f_0 and is given by

$$f_0 = \frac{1}{2\pi\sqrt{6}RC} = \frac{0.065}{RC}$$

At this frequency, the gain A must be at least 29.

That is,

$$\left|\frac{R_F}{R_1}\right| = 29$$

or $$R_F = 29R_1$$

For the loop gain β*A* to be greater than unity, the gain of the amplifier stage must be greater than 1/β or 29.

A > 29

2 Phase-shift Oscillator using FET:

Here an FET amplifier of conventional design is followed by three cascaded arrangements of a capacitor C and a resistor R, the output of the last RC combination being returned to the gate. If the loading of the phase-shift network on the amplifier can be neglected, the amplifier shifts by 180° the phase of any voltage which appears on the gate, and the network of resistors and capacitors shifts the phase by an additional amount. At some frequency the phase-shift introduced by the RC network will be precisely 180° and at this frequency the total phase-shift from the gate around the circuit and back to the gate will be exactly zero. This particular frequency will be the one at which the circuit will oscillate, provided that the magnitude of the amplification is sufficiently large.

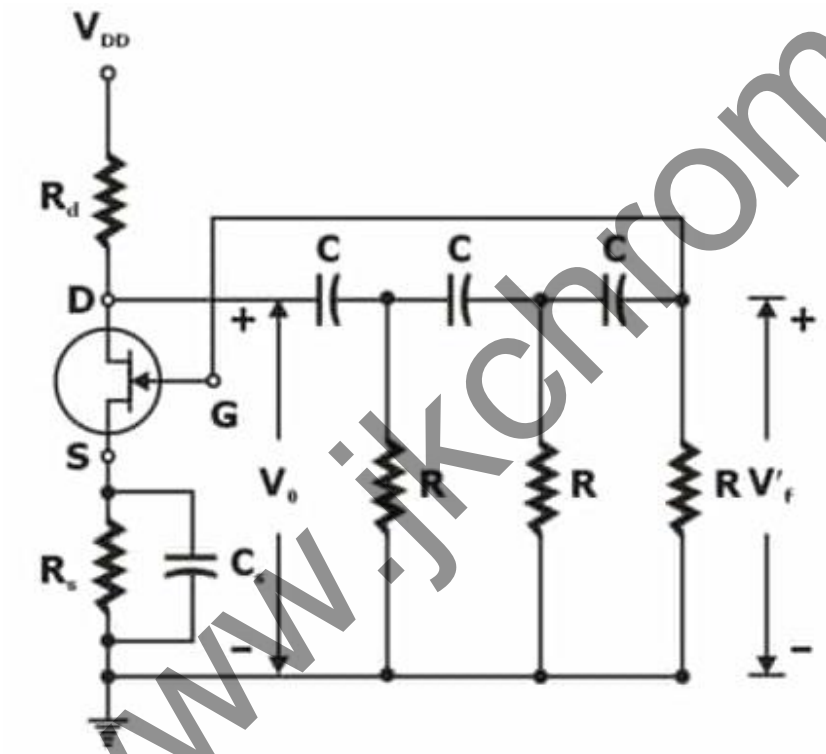


Figure 4: An FET Phase Shift Oscillator

The frequency of oscillation for this circuit is given by

$$\boxed{f = \frac{1}{2\pi RC\sqrt{6}}}$$

At the frequency of oscillation,

$$\boxed{\beta = +\frac{1}{29}}$$

In order that |βA| shall not be less than unity, it is required that |A| be at least 29. Hence and FET with μ < 29 cannot be made to oscillate in such a circuit.

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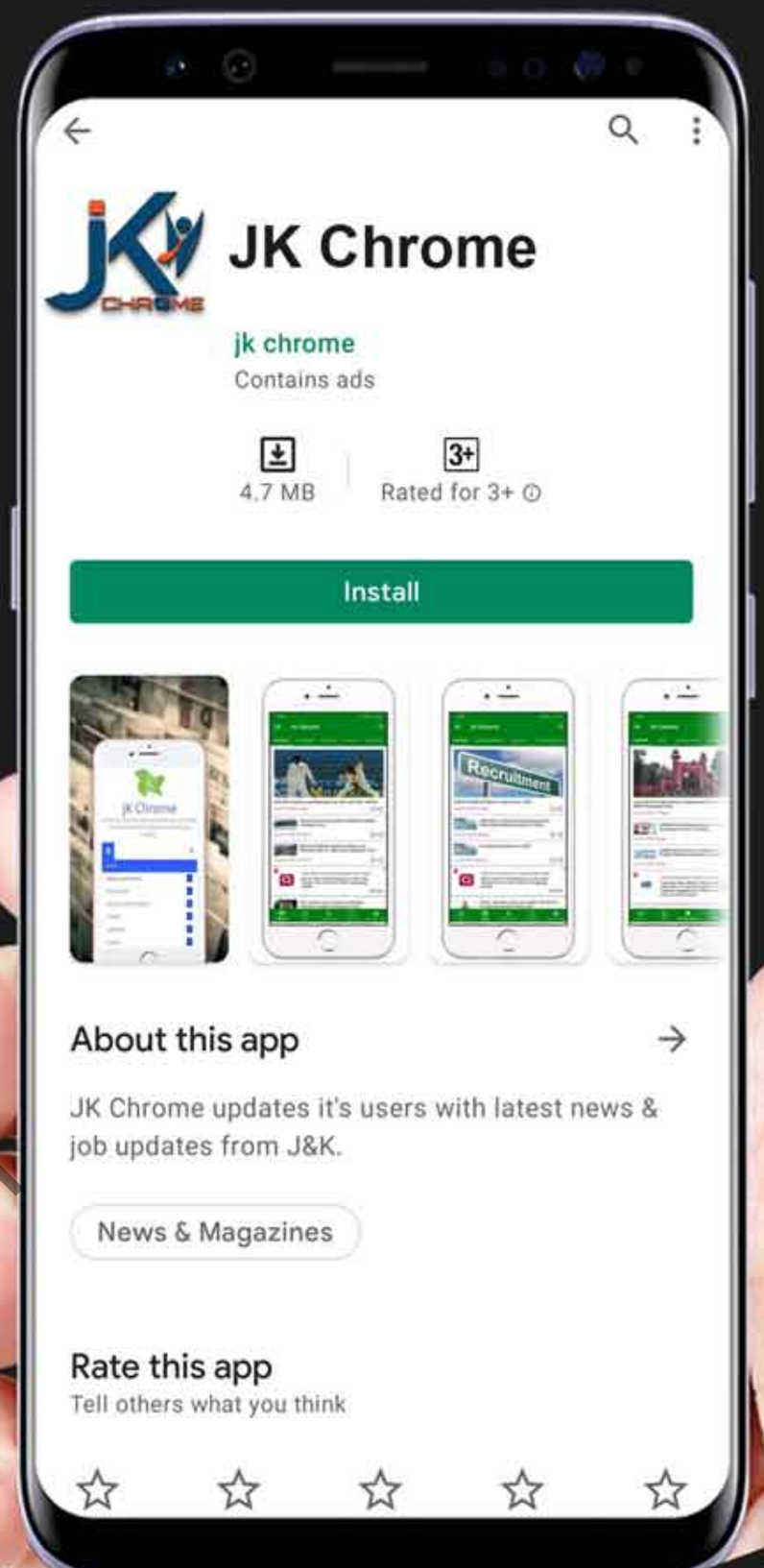

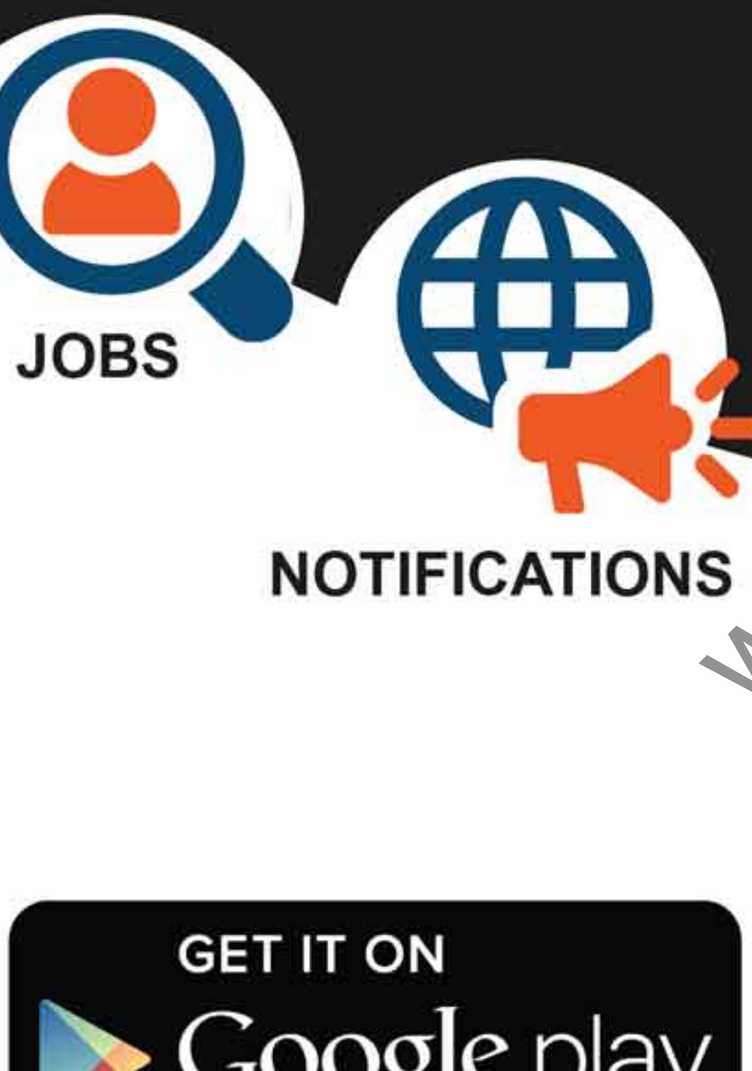

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